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55	+3P3V_LPS
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57	+5V_GPIO
58	+1P8V_+3P3V_PCH_GPPA
59	+1V_PCH
60	+1P2V_SFROC
61	+VPP
62	+1P2V_VDDQ
63	+VTT_DDR
64	+5V_MAIN & +3P3V_MAIN
65	+VCCIO
66	+VCCSA
67	+VCORE VGT CONTROLLER
68	+VCORE PHASE 1 & 2
69	+VCORE PHASE 3
70	+VGT Phase 1 & 2
71	USB POWER/FAN(Z2 Only)
72	Changelist

Intel SkyLake Plat f or m

SLK-S CPU / SLK PCH-H

BOM DISTRIBUTION RULE
Spitfire, Scorpion, Toledo, Bunun
(BOM,BOM,BOM, BOM)

DO NOT DISTRIBUTE


Marking	Description
I	Installed
NI	Not Installed
MP	Production Part ONLY
PROTO	Not For Production Part
CCL	Critical Components List

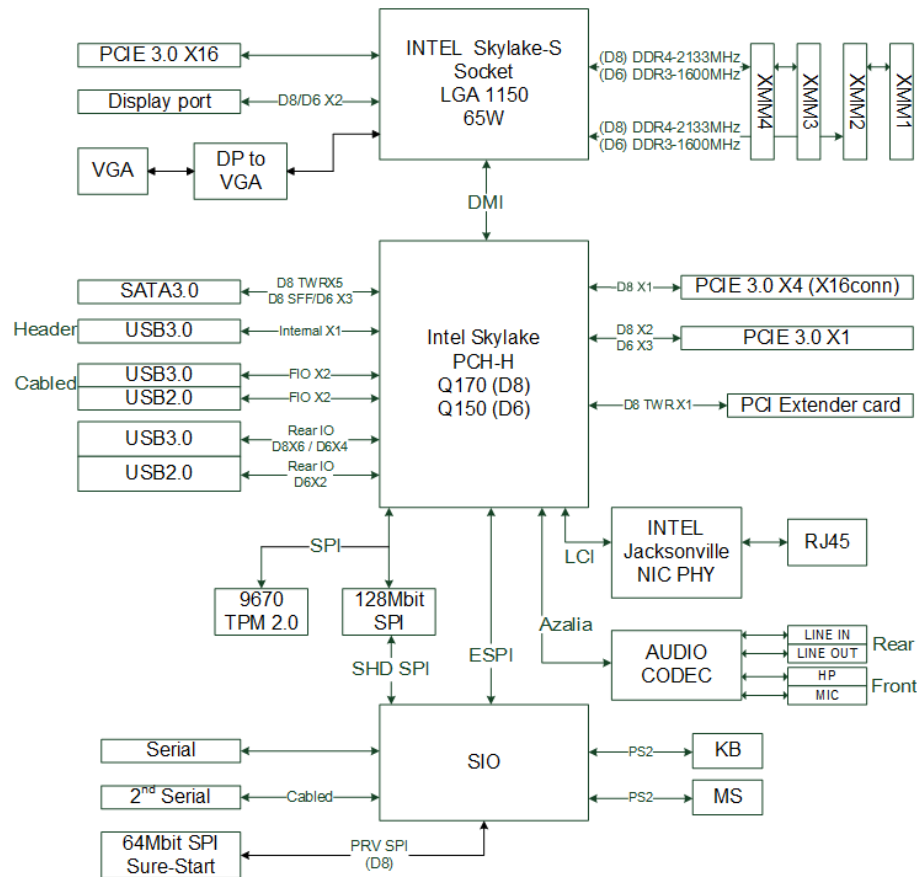
PCB AND SILKSCREEN COLOR		
Program Phase	Color of PCB	Silkscreen
DB1 (Design Build)	RED	YELLOW
DB2+	RED	WHITE
SI1 (System Integration)	LIGHT BLUE	YELLOW
SI2+	LIGHT BLUE	WHITE
PV1 (Production Validation)	GREEN	YELLOW
PV2+	GREEN	WHITE
MVB / PRODUCTION	GREEN	WHITE

	Spitfire	Scorpion	Toledo	Bunun
PCH	Q170	Q170	Q150	C236

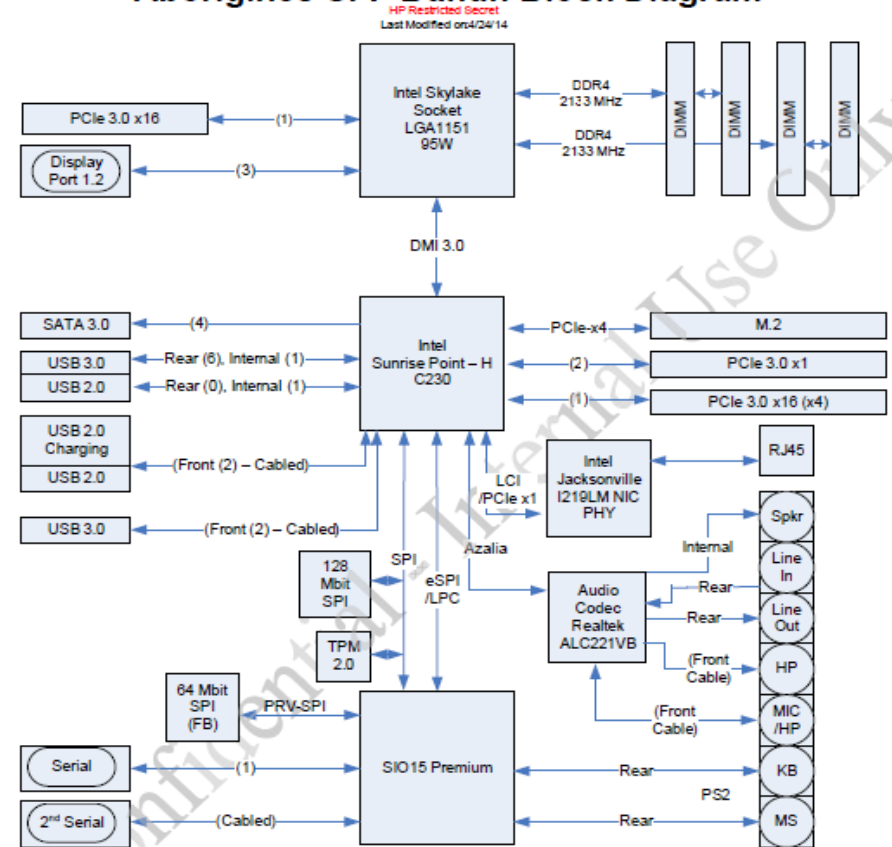
PCA P/N, Spitfire/Scorpion/Toledo/Bunun	795206-001/ 795206-002/ 795231-001/ 795003-001
SCH P/N, Spitfire/Scorpion/Toledo/Bunun	795207-000/ 795207-000/ 795207-000/ 795207-000
PCB P/N, Spitfire/Scorpion/Toledo/Bunun	795208-001/ 795208-001/ 795208-001/ 795208-001

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Aborigines SFF Bunun Block Diagram

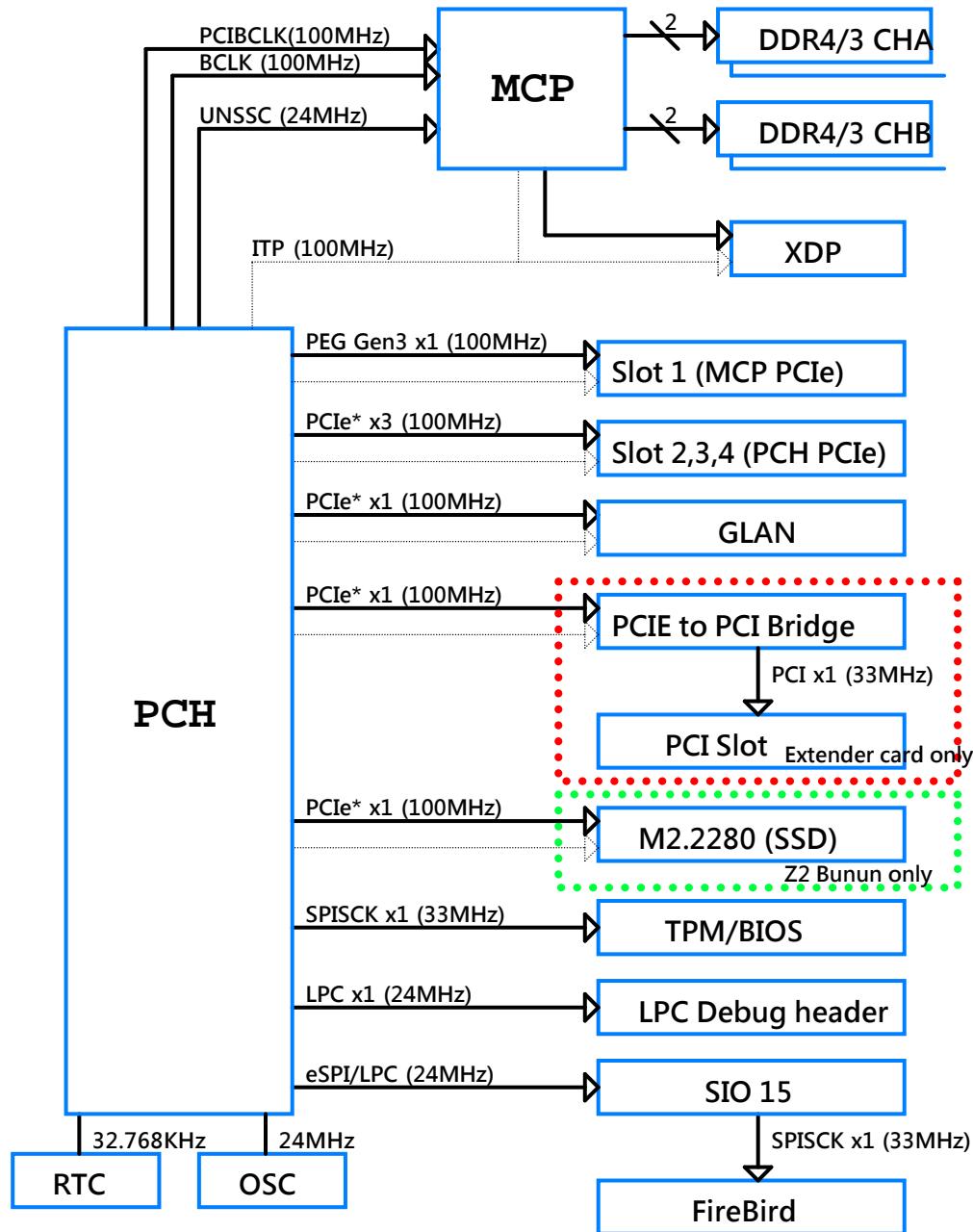


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Clock Diagram



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POWER SUPPLY

+12V_CPU
+12V
-12V
+12V_AUX

VBAT 3.0
VCCRTC

+12V_CPU
+12V_CPU
+12V_DAUL
BATT1

CPU Core Switcher
3+2phase Switching
+VCCIA 63A 0V - 1.52V
+VCCGT 37A 0V - 1.52V

VCCSA Switcher
11A 1.05V

VCCIO Switcher
5.5A 0.95V

VCC_DDR Switcher
12.14A 1.2V

+VPP
2.24A 2.5V

+1.0V_PCH
10.66A 1.0V

+1P8V_+3P3V_PCH_GPPA Switcher
0.4A 1.8V

5V & 3.3V Switcher
+5V_AUX
14.462A
+3P3V_AUX
17.16

+3.3V_LPS
0.502A (LPS:0.00206A)

DDR4 DIMM x4
+VDDQ 12A 14.4W
+VPP 1A 0.6W

AUDIO
+5V_AUX 33mA
+3.3V_AUX 33mA

SPI EEPROM
+3.3V_AUX 30mA 0.1W

LAN
+3.3V_LAN 542mW

+VCCIA
+VCCGT

+VCCSA

+VCCIO

+VDDQ

+VPP

+1.0V_AUX

PIV8_P3V3_PCH_GPPA

+5V_AUX/+5V_DUAL/+5V_MAIN/+5V_GPIO

+3P3V_AUX/+3P3V_MAIN

+3.3V_LPS

DDR LDO
0.75A
+VTT

PARALLEL PORT
+5V 15mA 75mW

SERIAL PORT
+12V 1mA 12mW
+3P3V_AUX 50uA 165uW

PS2 KB/M
+5V_DUAL 50mA 250mW

PCIE SLOT x4
+3.3V_AUX 0.375A 1.2375W
+3.3V_MAIN 9A 29.7W
+12V 9.7A 116.4W

USB PORT x11
+5V_DUAL 3.0 X9 2.0 X2
9.1A 45.5W

SLK (65W TDP)
+VCCIA 79A
+VCCGT 45A
+VCCSA 11.1A
+VCCIO 5.5A

SKL-S (5.92W TDP)
+1.0V_AUX 9.948A 9.948W
PIV8_P3V3_PCH_GPPA 0.038A 0.0684W
+3.3V_AUX 0.633A 2.0889W
+3.3V_LPS 0.204A 0.6732W
+3P3V_MAIN 7mA 23.1mW
+3V_BATT 1mA 3.3mW


SUPER I/O
+3.3V_AUX 95mA 313.5mW
+3V_BATT 1.5uA 3.3uW
+3.3V_LPS 10uA 33uW
+SIO_SPI_POWER 30mA 99mW
+IP0V_VCCST 10mA 10mW
PIV8_P3V3_PCH_GPPA 10mA 33mW

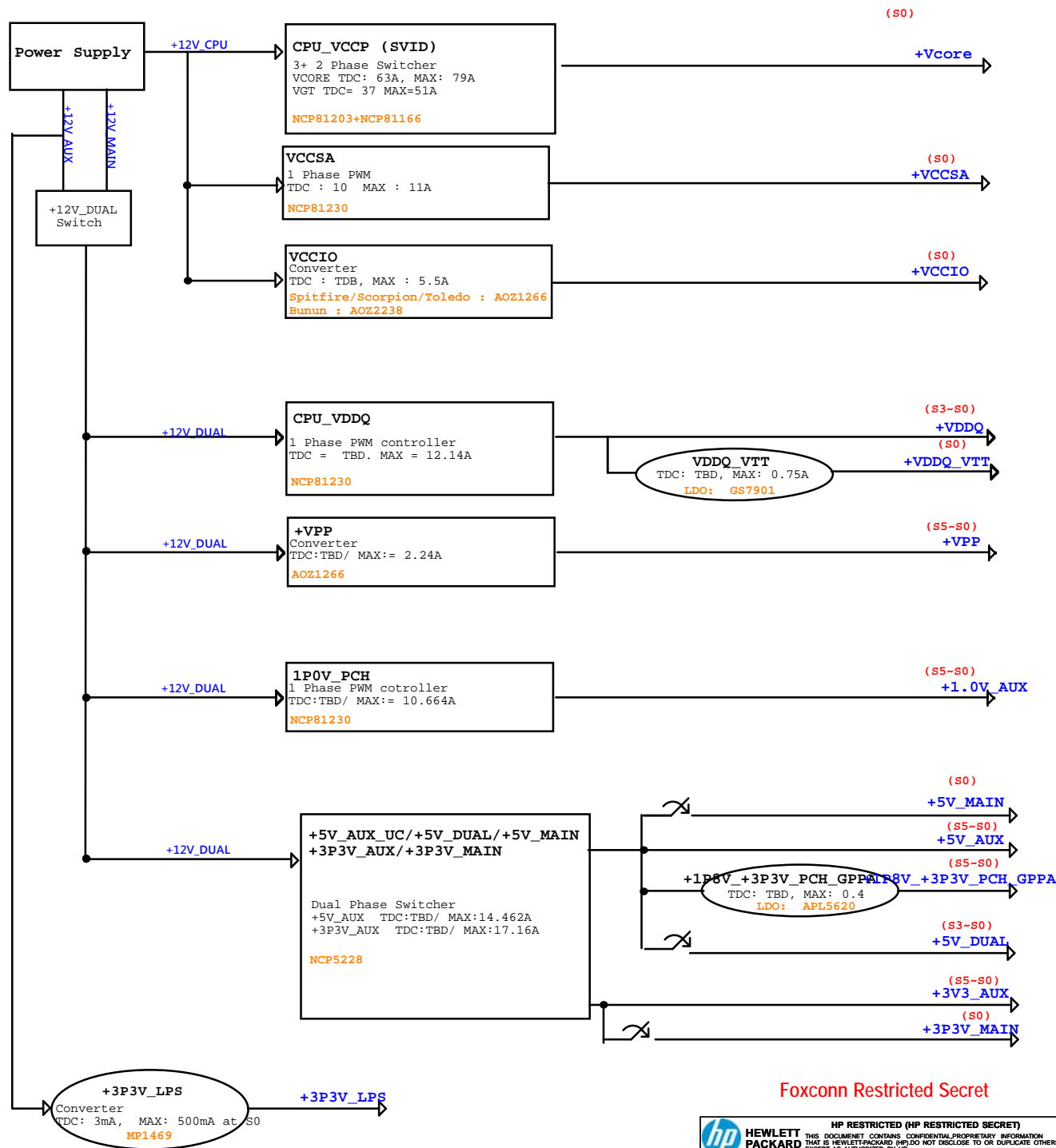
HARD DRIVER
+12V 0.35A 4.2W
+5V 0.72A 3.6W

CD ROM
+12V 1.5A 18W
+5V 1.5A 7.5W

FAN
+12V 200mA 2.4W

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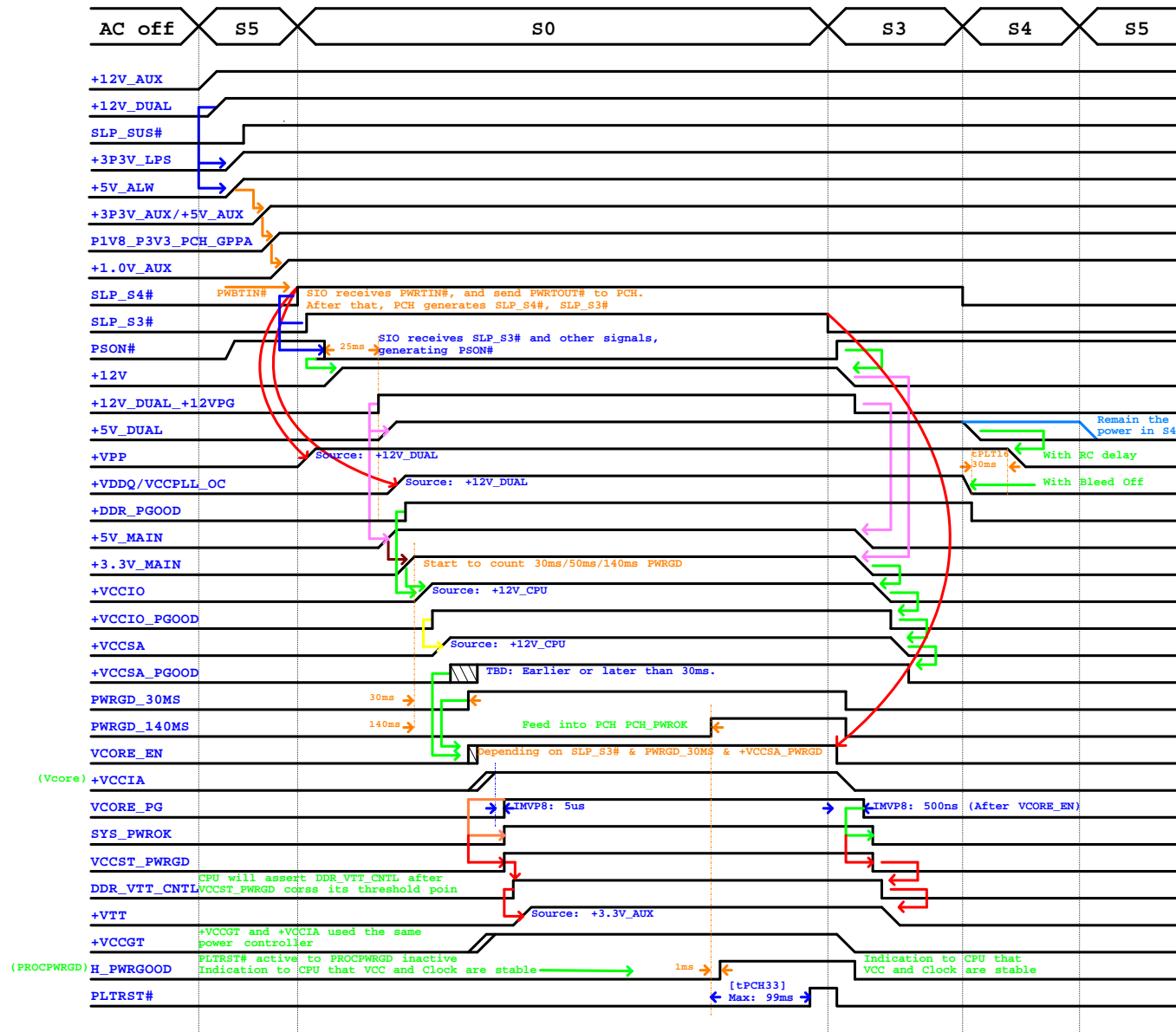
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POWER SEQUENCE DIAGRAM



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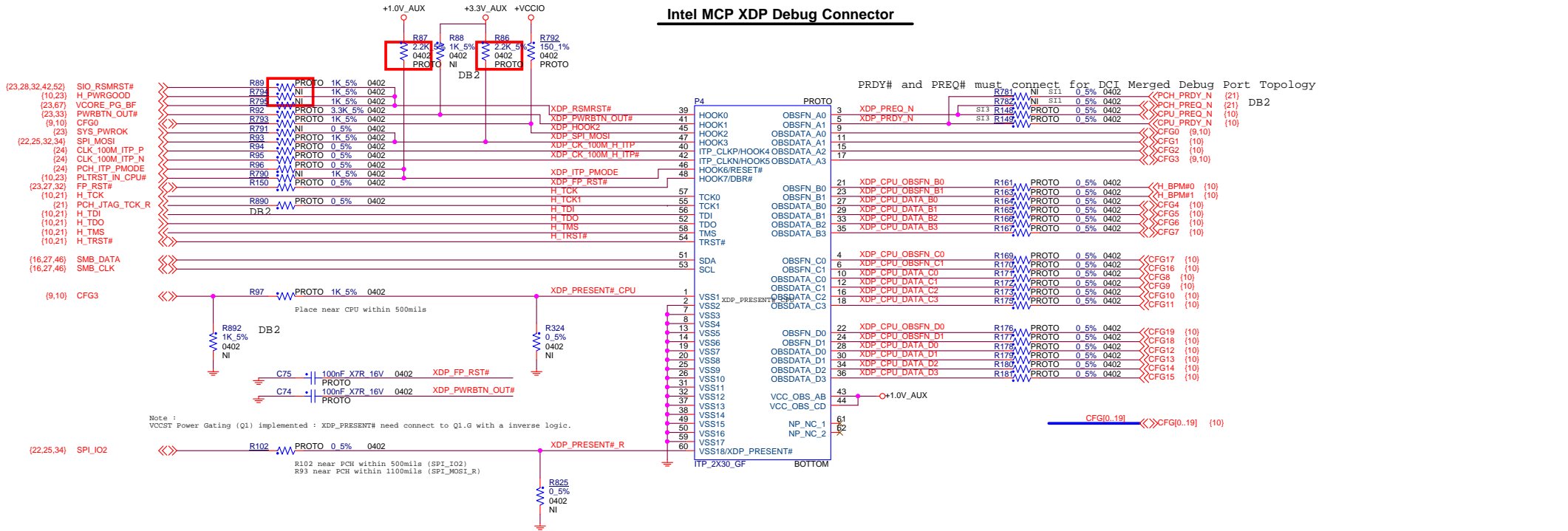
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Title: POWER SEQUENCE DIAGRAM			
Size: C	Document Number: 795207-000	Rev: A	
Date: Monday, June 29, 2015		Sheet: 7	of 72

SPITFIRE




Change list from XDP to CDI:
NI: R890/R796
I: R880/R881/R882/R883/R884/R885/R781/R782

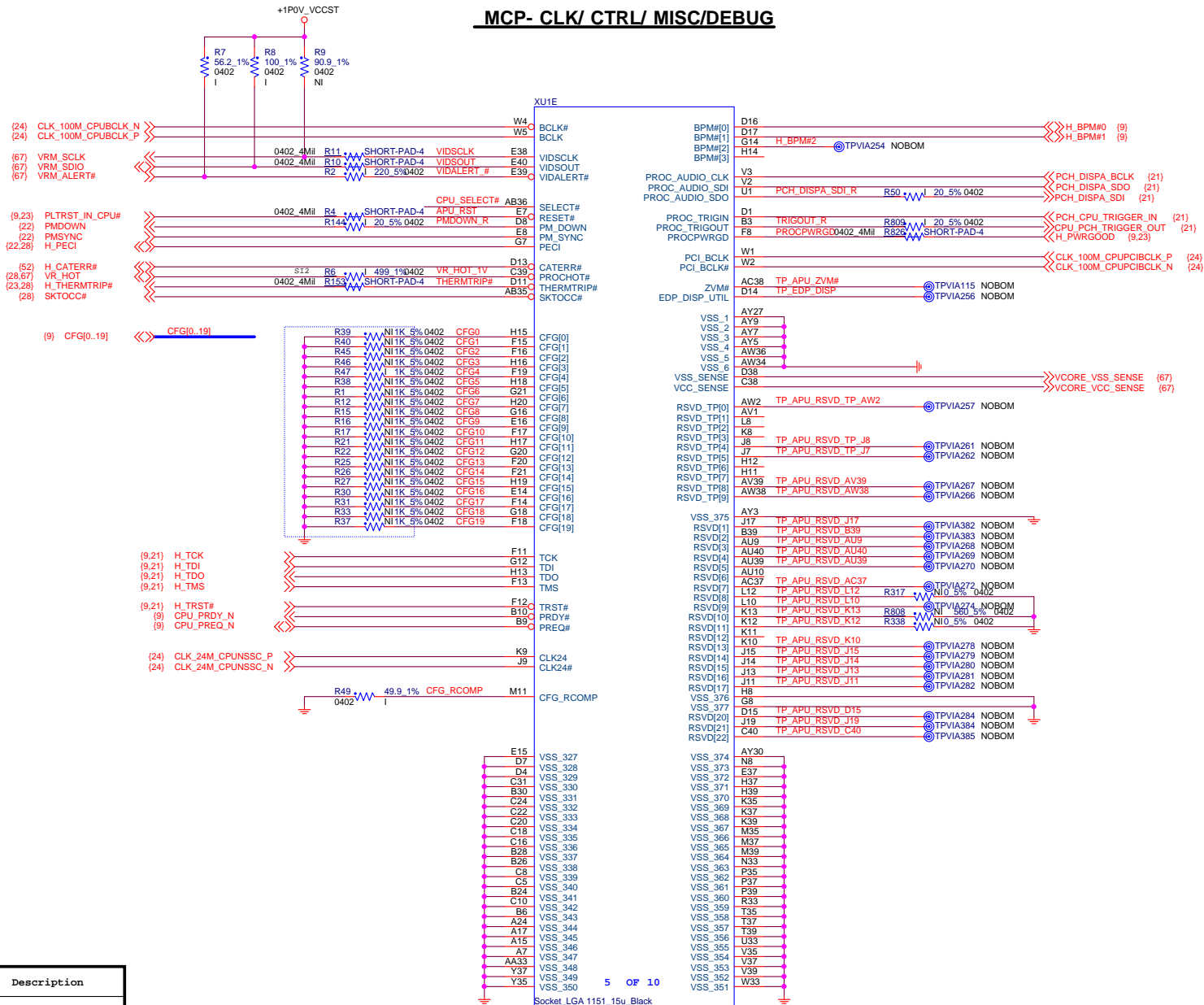
Intel MCP XDP Debug Connector



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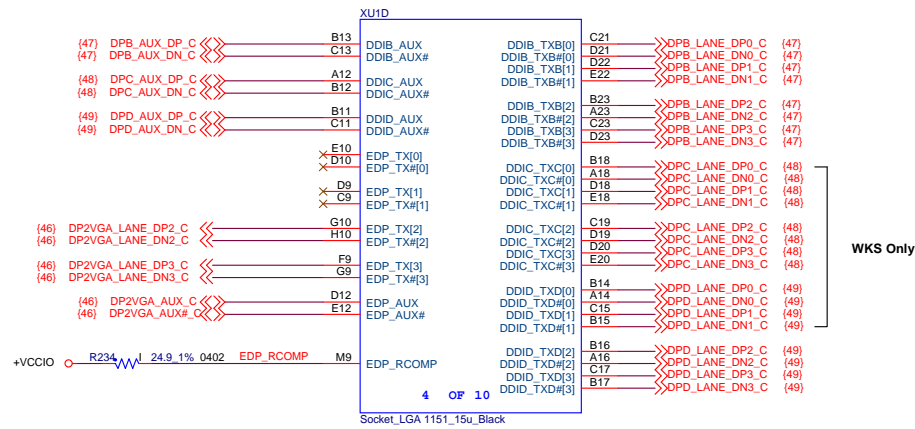
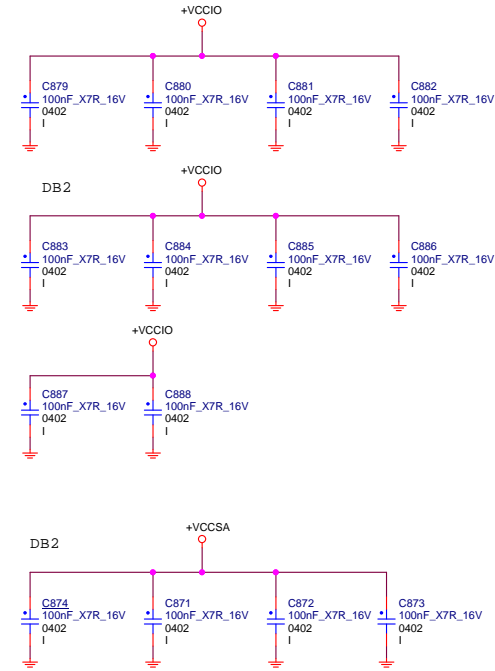
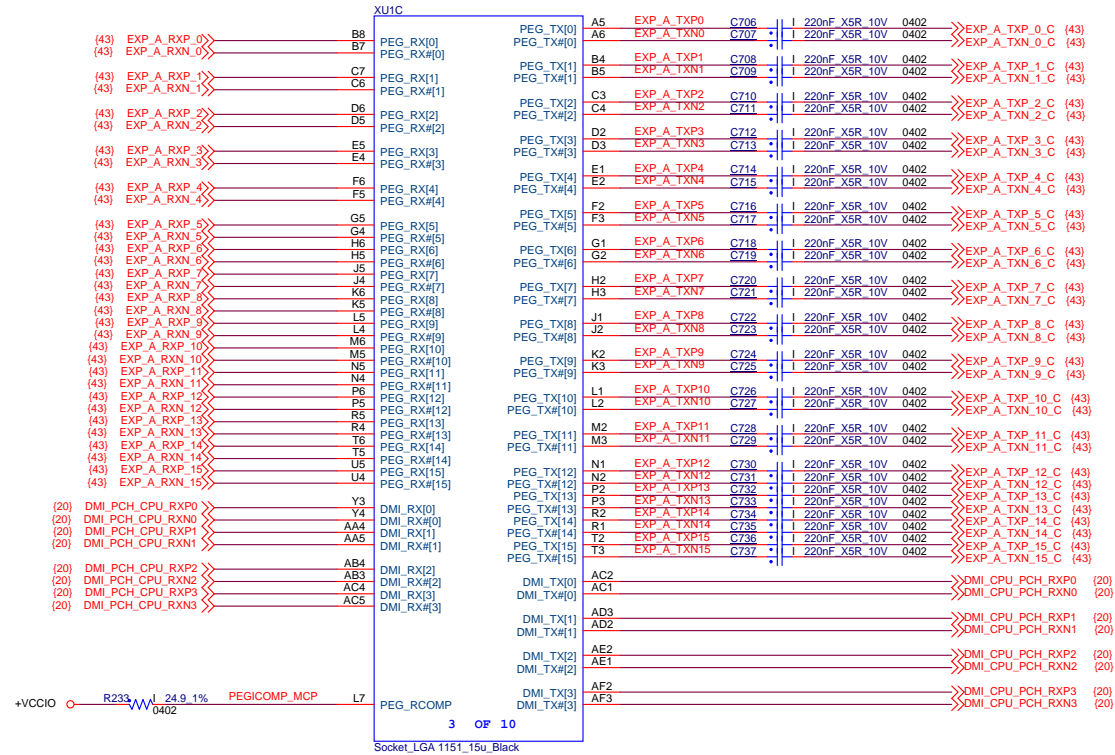
MCP- CLK/ CTRL/ MISC/DEBUG



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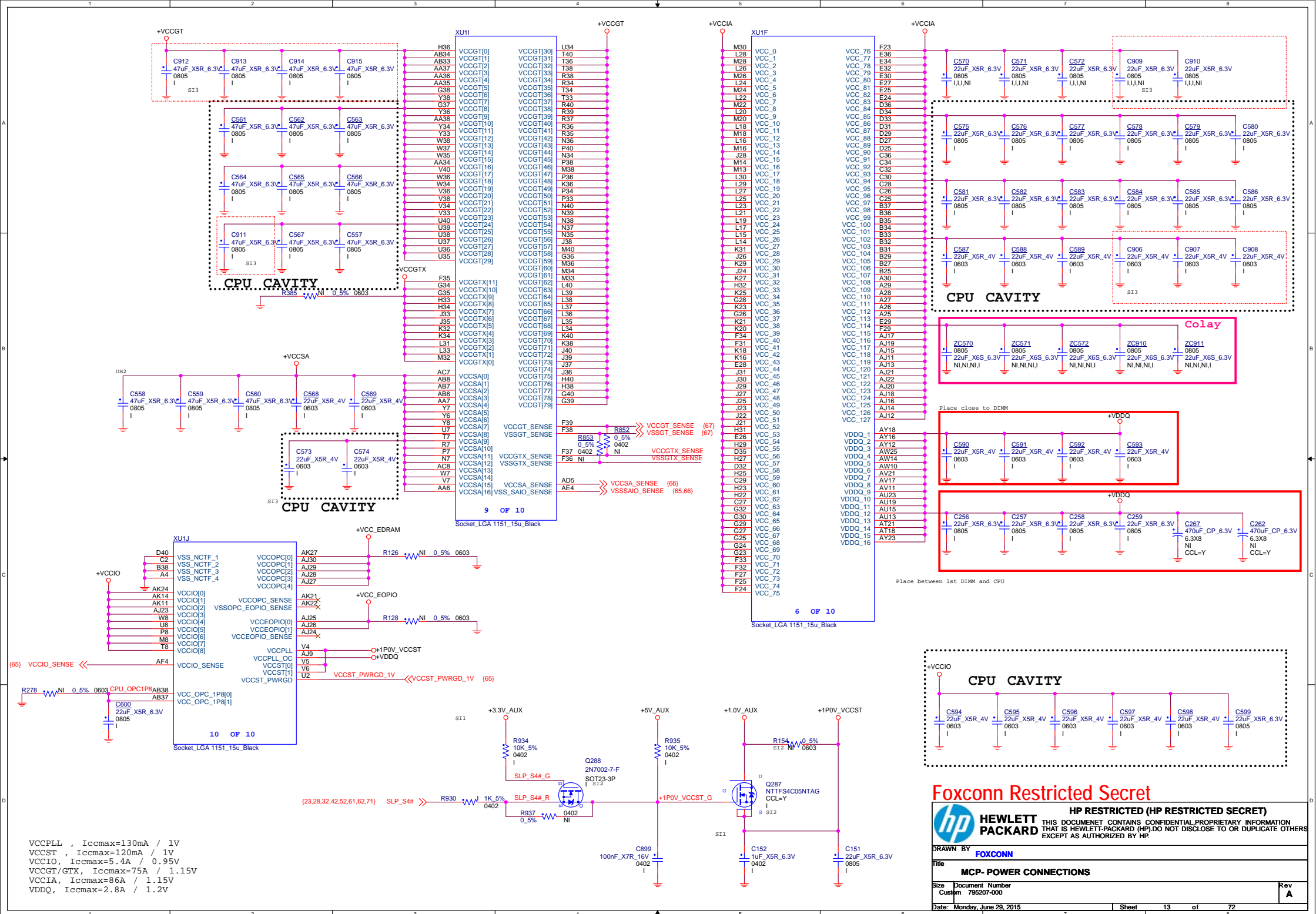
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Size Document Number Custom 795207-000	Rev A
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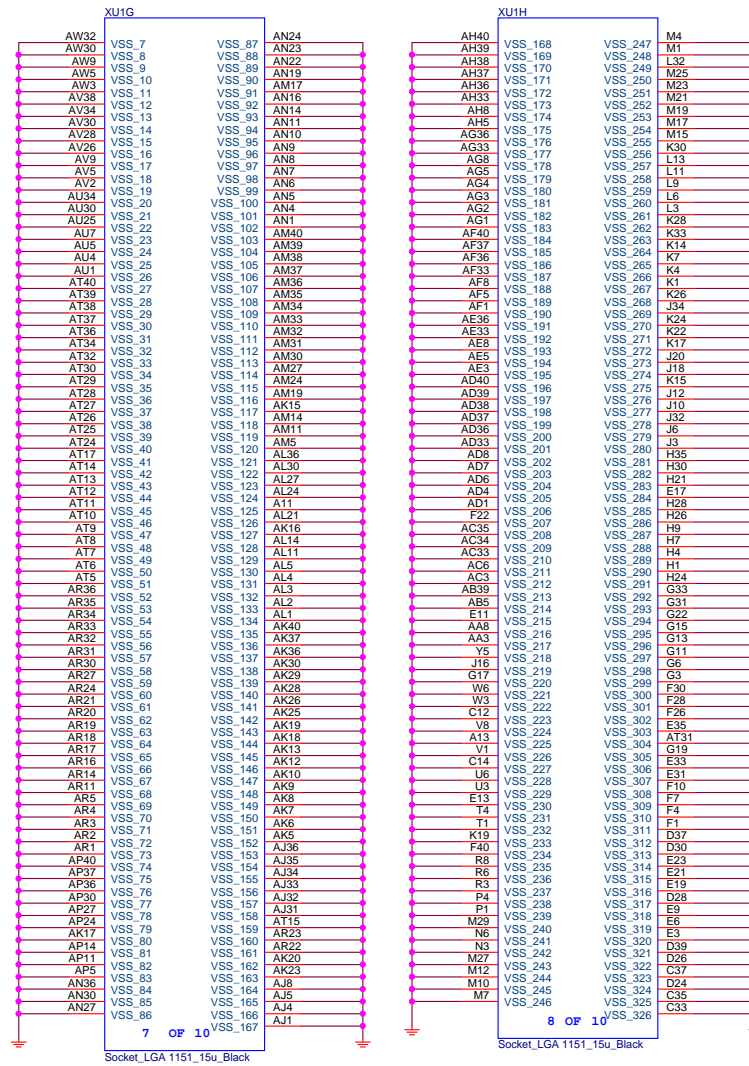
MCP - PCIE,DMI,FDI,DDI




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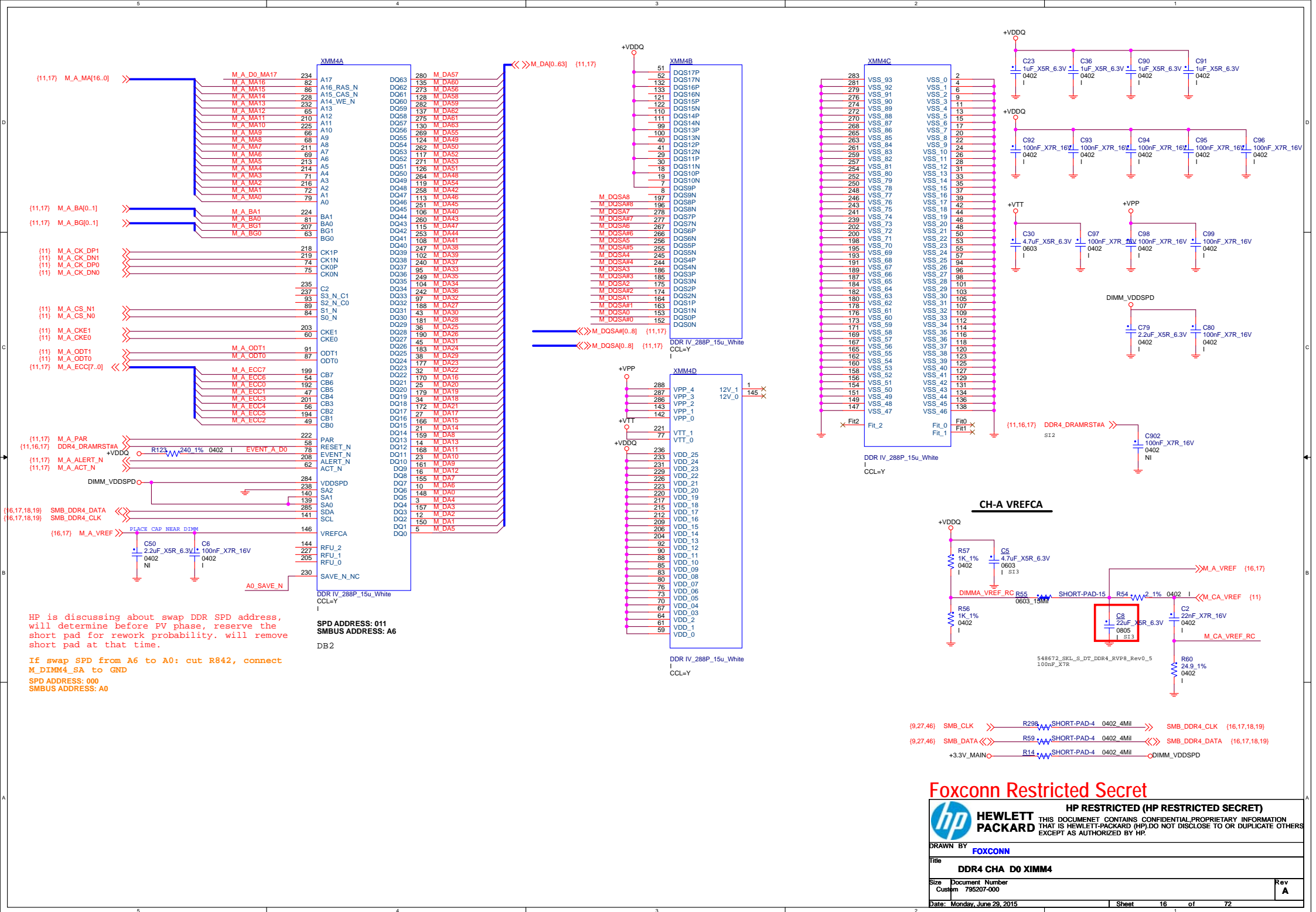
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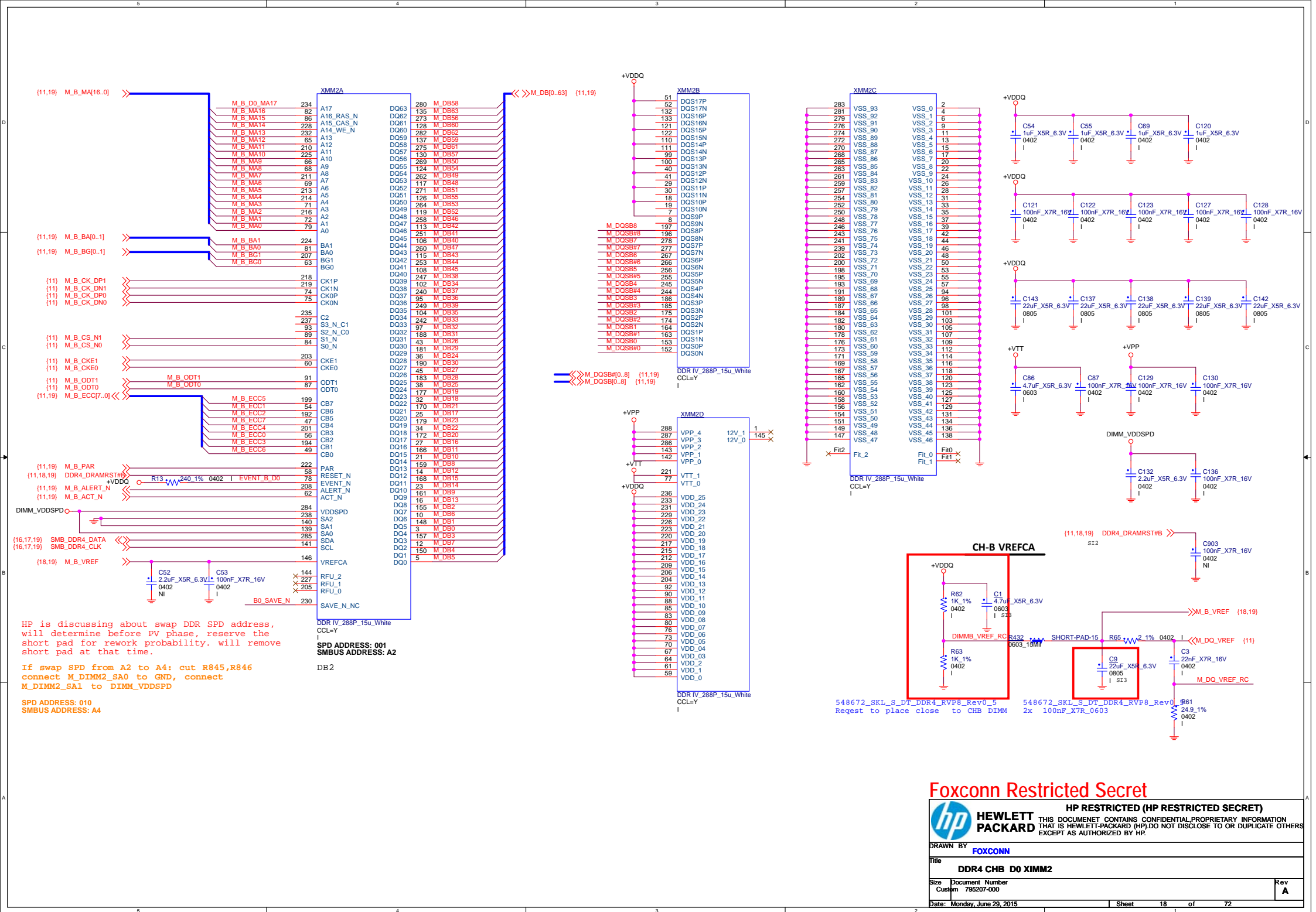
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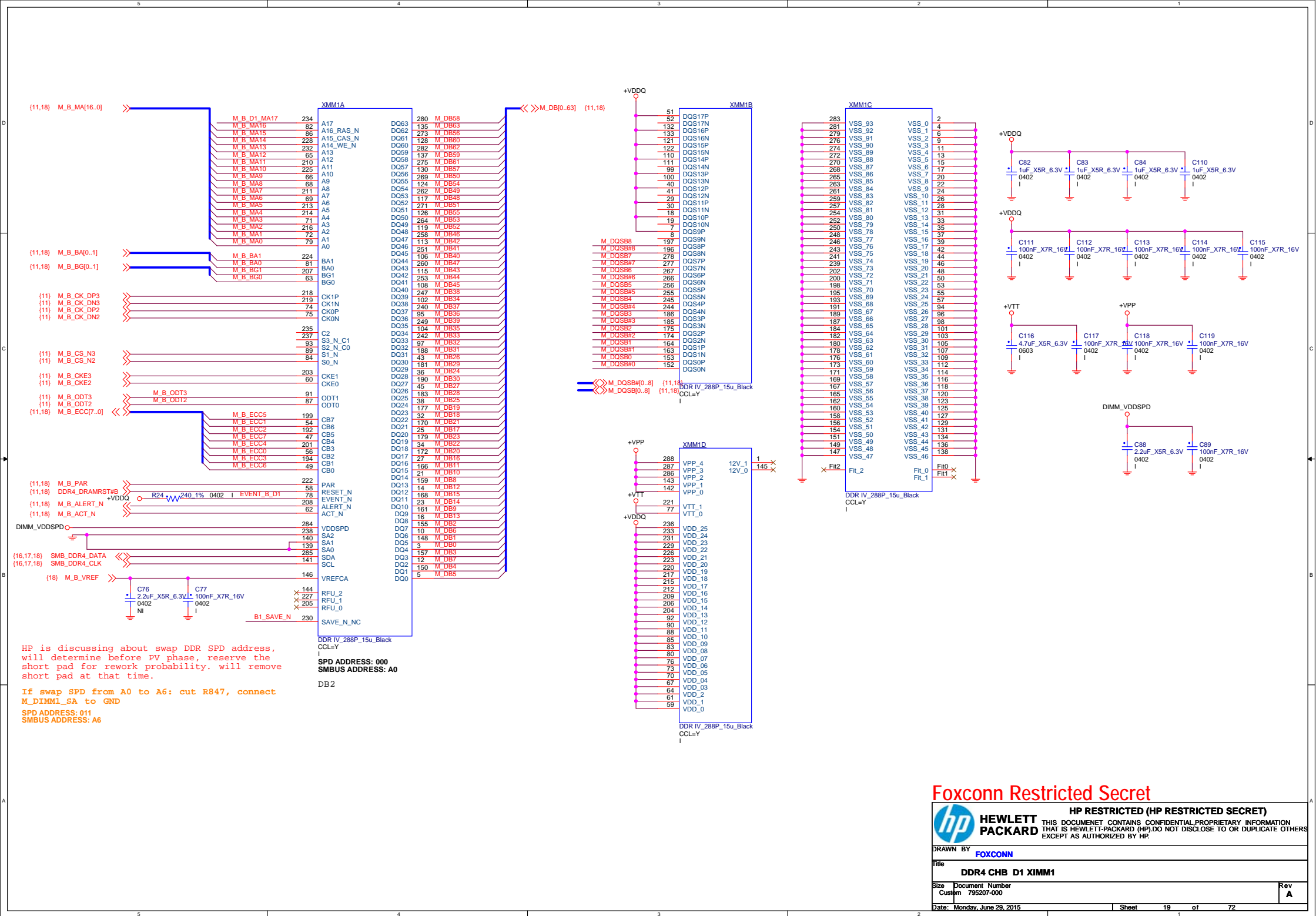


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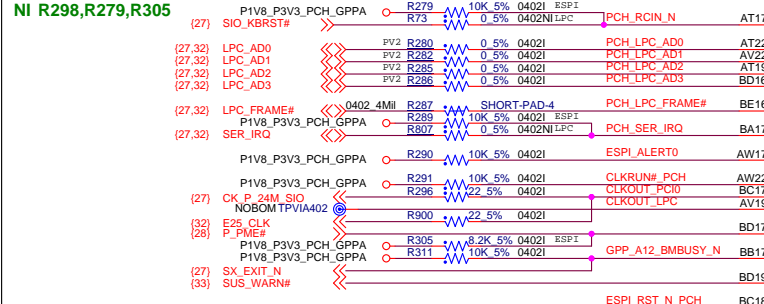
(38) SATA_RXN0
(38) SATA_RXP0
(38) SATA_TXN0
(38) SATA_TXP0
(38) SATA_RXN1
(38) SATA_RXP1
(38) SATA_TXN1
(38) SATA_TXP1
(38) SATA_RXN2
(38) SATA_RXP2
(38) SATA_TXN2
(38) SATA_TXP2
(38) SATA_RXN3
(38) SATA_RXP3
(38) SATA_TXN3
(38) SATA_TXP3
(29) PCH_HSIN17
(29) PCH_HSON17
(29) PCH_HSOP17
(29,38) SATA_RXN4_PCIE_HSIN18
(29,38) SATA_RXP4_PCIE_HSIP18
(29,38) SATA_TXN4_PCIE_HSON18
(29,38) SATA_TXP4_PCIE_HSOP18
(29) PCH_HSIN19
(29) PCH_HSIP19
(29) PCH_HSON19
(29) PCH_HSOP19
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(29) PCH_HSOP20

(29) M2_DEVSLP

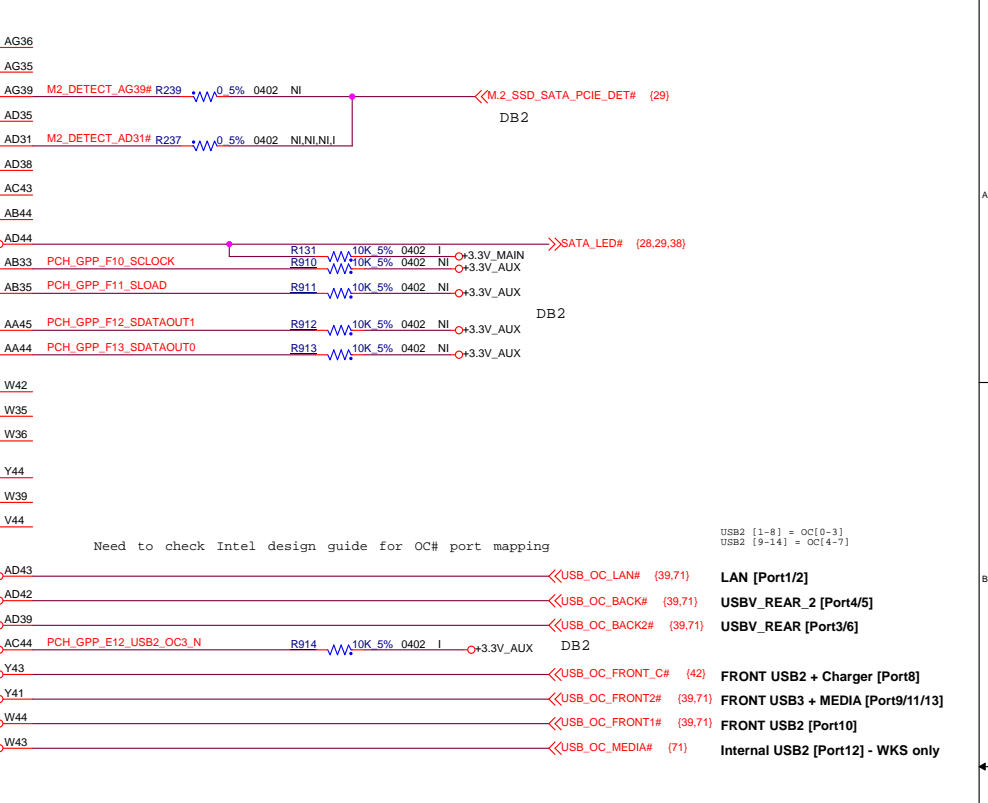
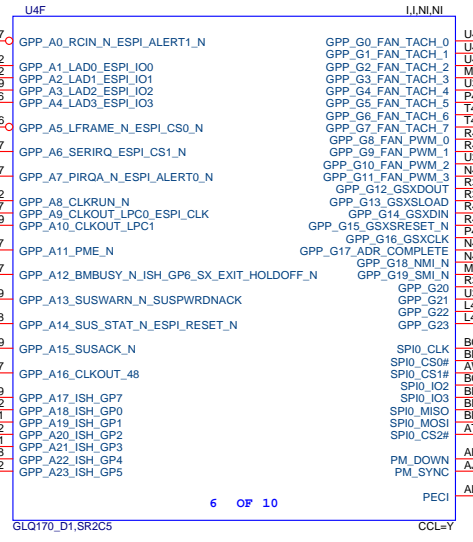
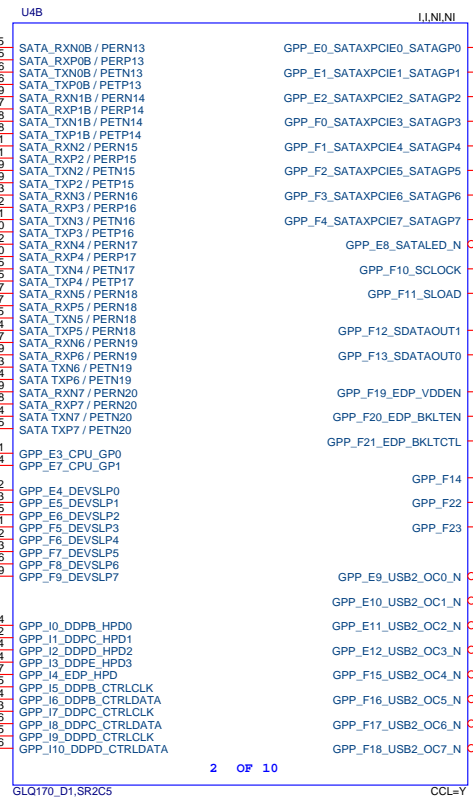
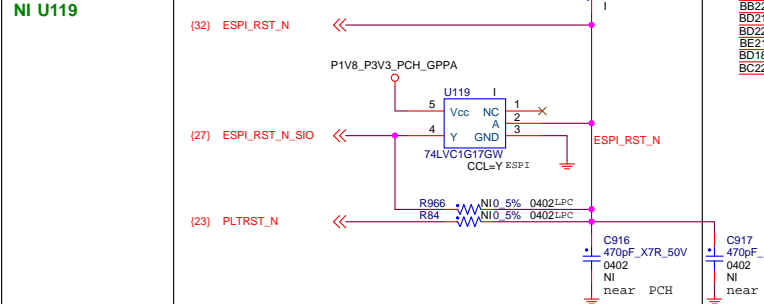
(47) DPB_HPD_R
(48) DPC_HPD_R
(49) DPD_HPD_R
(46) EPD_HPD_R

(47) DDPB_CTRLCLK
(47) DDPB_CTRLDATA
(48) DDPB_CTRLCLK
(48) DDPB_CTRLDATA
(49) DDPD_CTRLCLK
(49) DDPD_CTRLDATA

LPC mode : I R807,R73
NI R298,R279,R305



LPC mode : I R84,R966
NI U119



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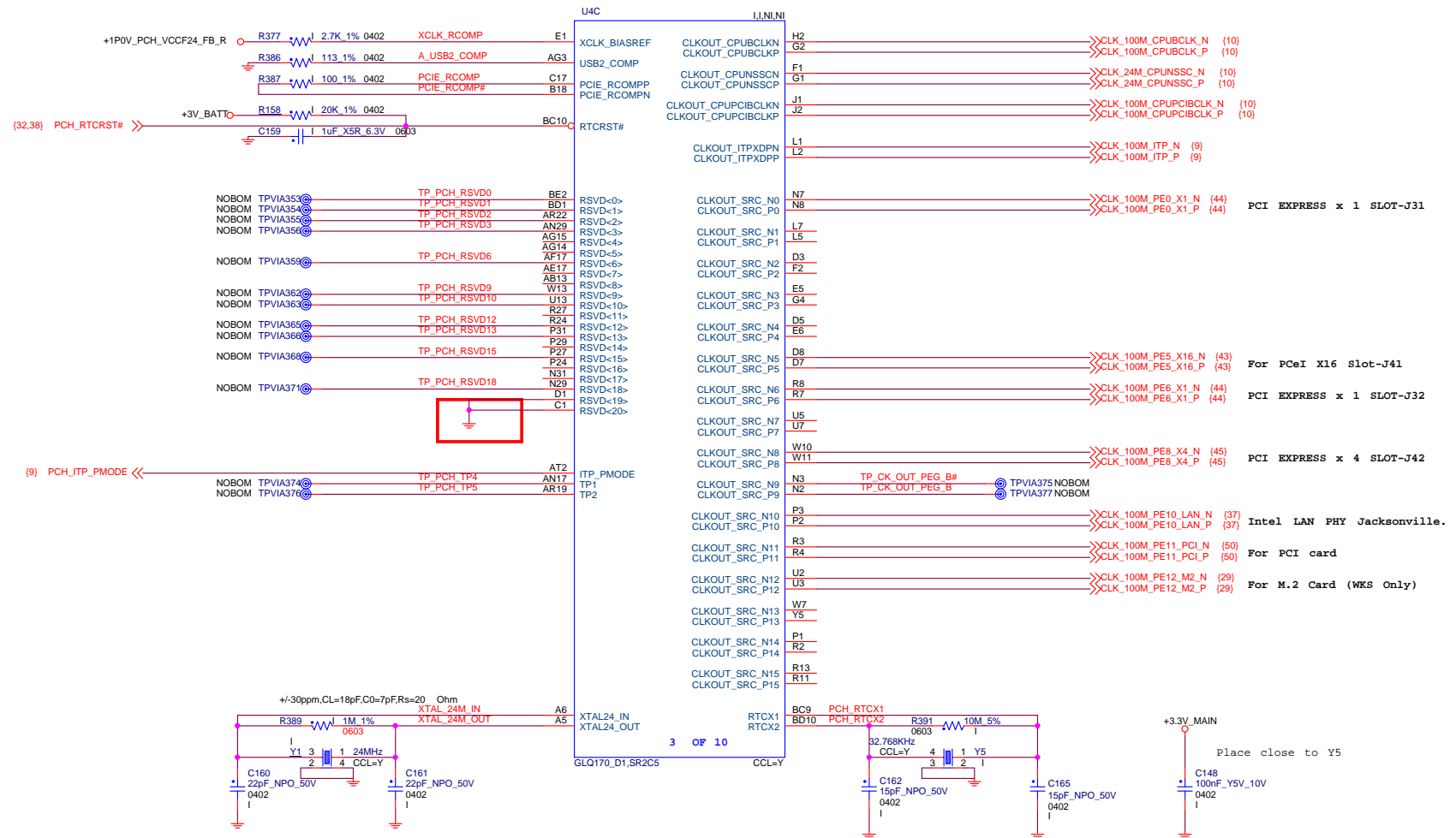
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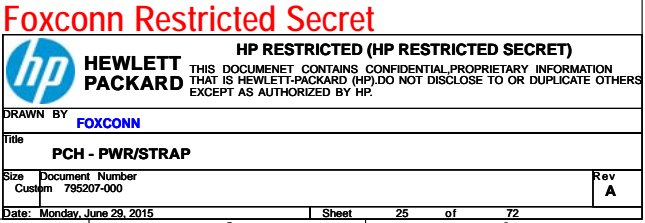
Rev: **A**

PCH - CLOCK DISTRIBUTION



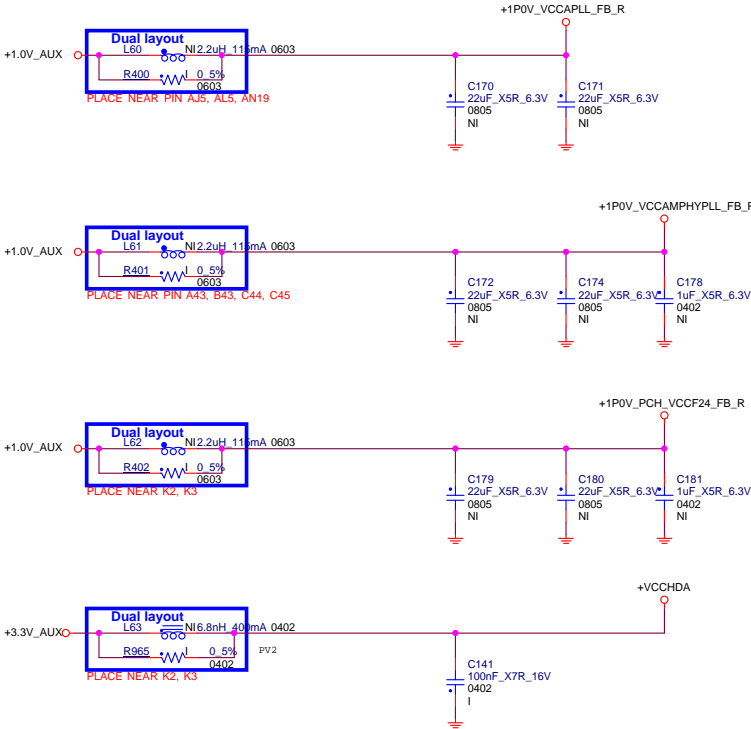
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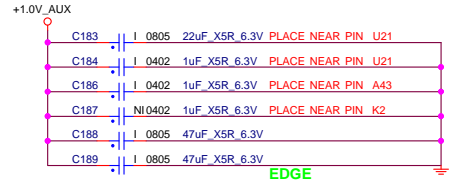


SKYLAKE Decoupling & filter

FILTER



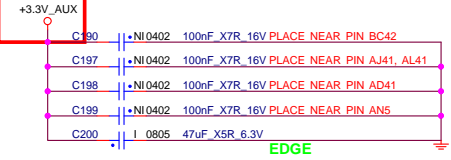
V1.0A



V3.3 DSW



V1.8A / V3.3A



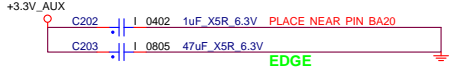
VccPGPPA



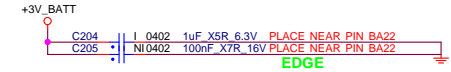
V1.8A / V1.8S / V3.3S



V3.3A



VCCRTC




Power Plane Isolation

Need to update for SLK

Voltage	Interface	PCH Pins sharing power rail
VCC_PCH 1.05V	Core	U26, U25, U23, U21, V26,
	PCIe/SATA/ USB3	T19, T20, F22, P23, P25, F26, P28, P14, P16, P17
	GPIO/LPC	AC12
	FDI	M14
	DIFFCLK	U12, V14 W14 AB2
	SSC	T16, V16 AA16, W16
	USB2	AF19, AF20, AF22, AF23, AP22
PCH 3.3V Standby	SUS	AM33, AN33
	USB2	AH18, AH20, AH22, AJ20, AK20
	AZALIA	AW26
	USB3	P20
	RTC	AP35
PCH 3.3V	CLK	AM7, AM9, AP5, AP7, AR4, AT5, AV4, AW4, AW9, AG12, AK11,
	HVCMOS	AG1
	PCIe	AV3, AW3
	Core	U30, W30
	Fuse	AF26

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Title
PCH-PLL FILTER & DECOUPLING

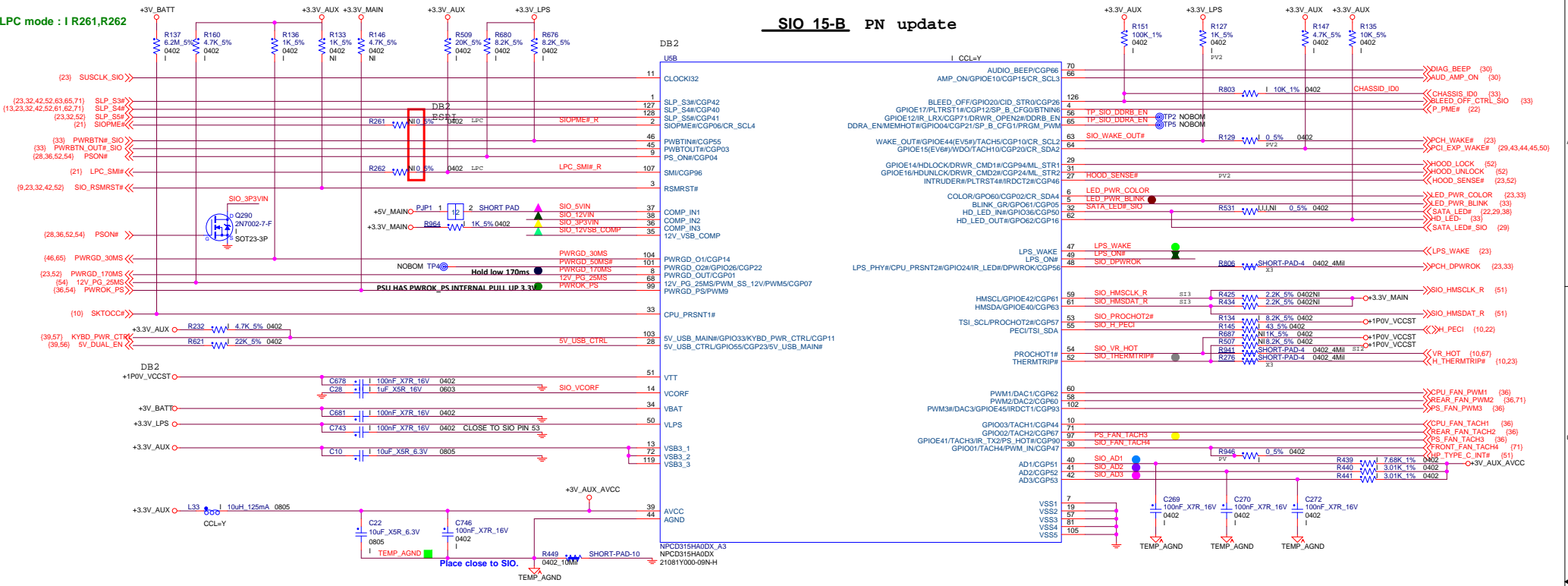
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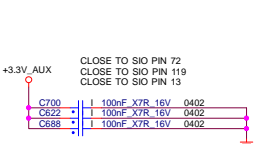
Rev
A

LPC mode : I R261,R262



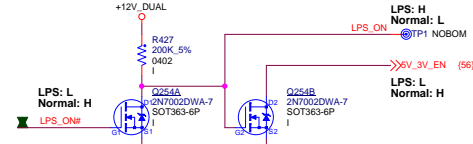
SIO 15-B PN update

SIO15- SIO Input Power Decoupling Cap

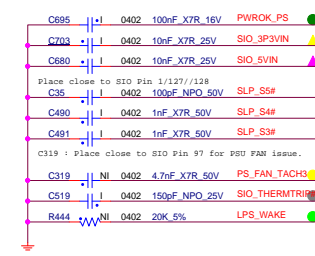


LPS ON# / LPS_ON

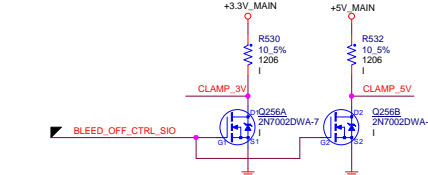
When LPS_ON# is asserted, the regular standby power rail is turned off and the small standby power well is activated.



SIO15- SIO Critical Signal PU/PD + Decoupling

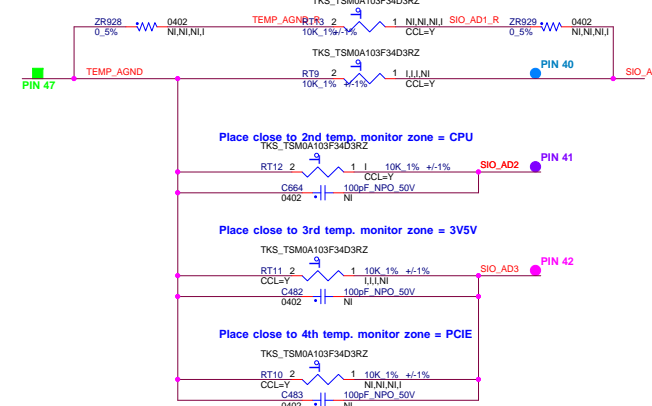


BLEED OFF 3.3V / 5V

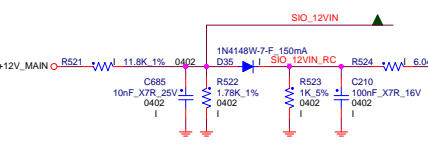


THERMAL SENSORS (SIO15)

Place close to Ambient temp. monitor zone=Ambient



COMPARATOR INPUT 2 - 12V



Foxconn Restricted Secret

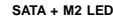
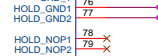
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DATE: Monday, June 28, 2015

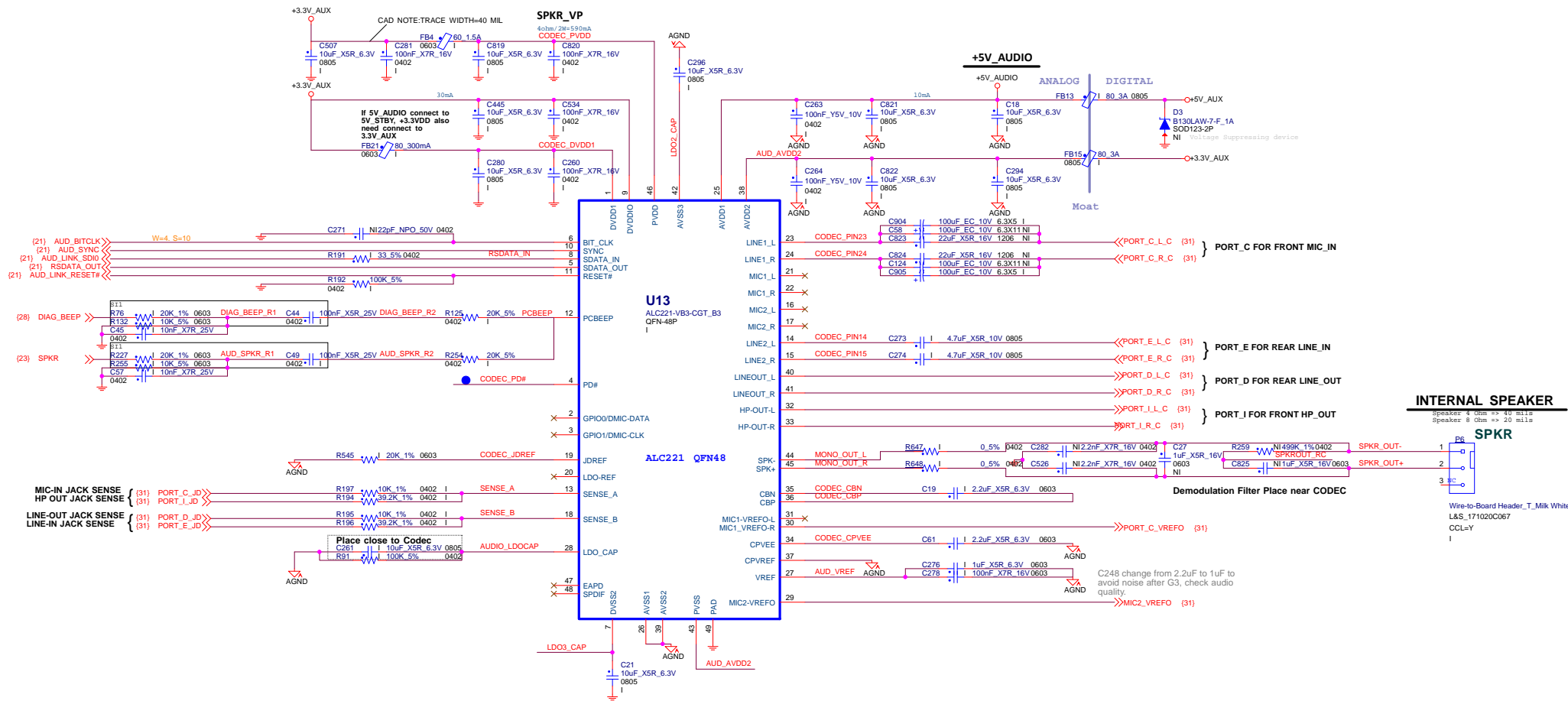
Sheet 28 of 72

M.2 SOCKET3 / KEY M

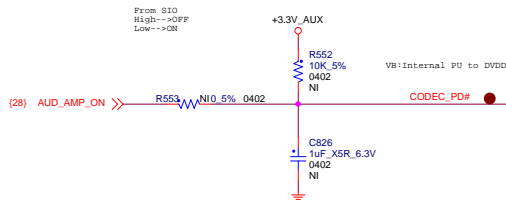


BOM DISTRIBUTION RULE
Spitfire, Scorpion, Toledo, Z2
(BOM,BOM,BOM, BOM)

HD AUDIO CODEC



CODEC_PD# CONTROL CIRCUIT



Note :

Retasking Function

1. Front IO - Microphone + Headphone
2. Front IO - Microphone + LinIN
3. Rear IO - LineIn + MicronPhone

PortC: MIC_IN(Default) + LineIn + HP

BOM DISTRIBUTION RULE
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Size	Document Number	Rev A	
Custom	795207-000		
Date: Monday, June 29, 2015	Sheet	30	of 72

REAR AUDIO HEADER

PORT_E FOR REAR LINE_IN


PORT_D FOR REAR LINE_OUT

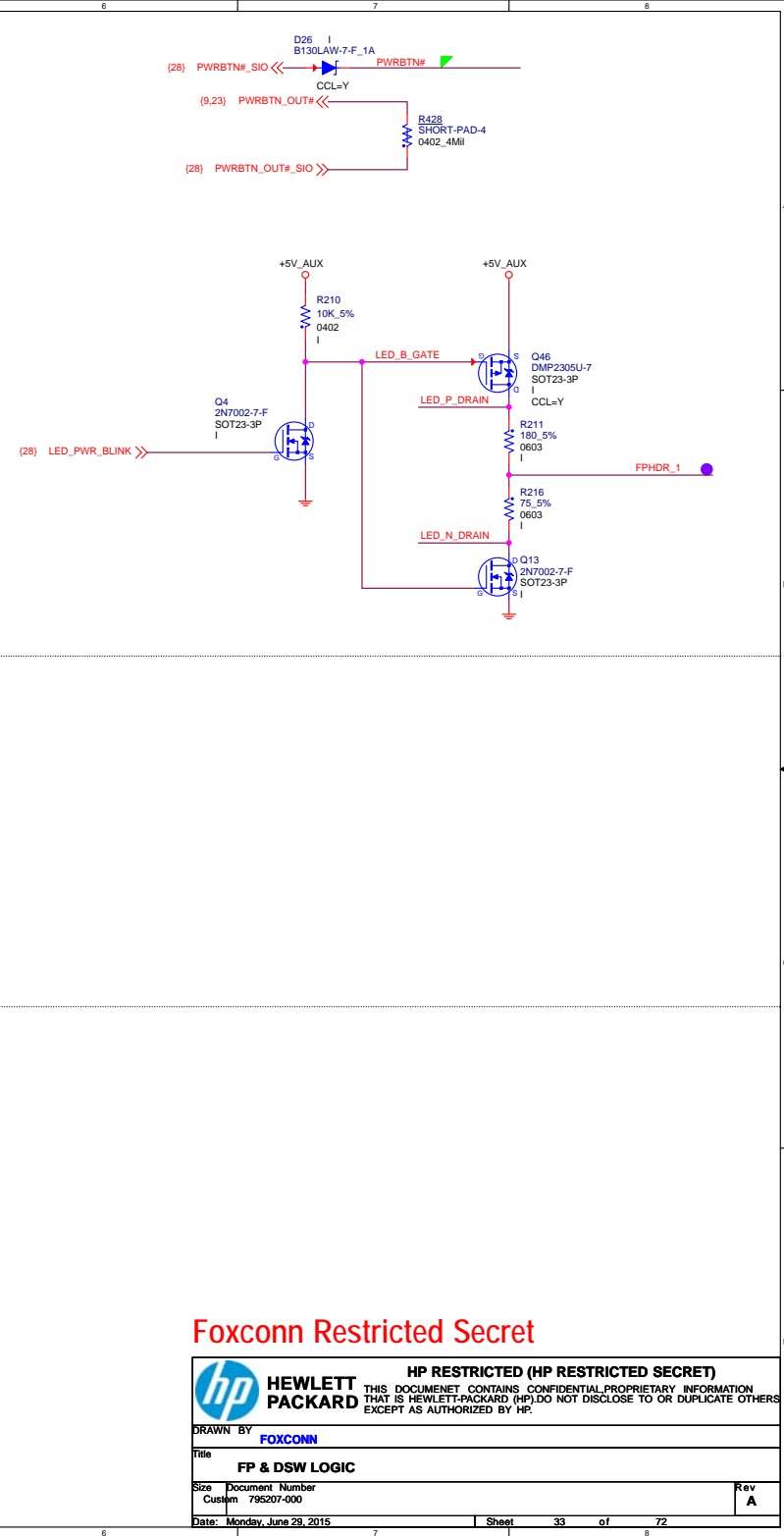
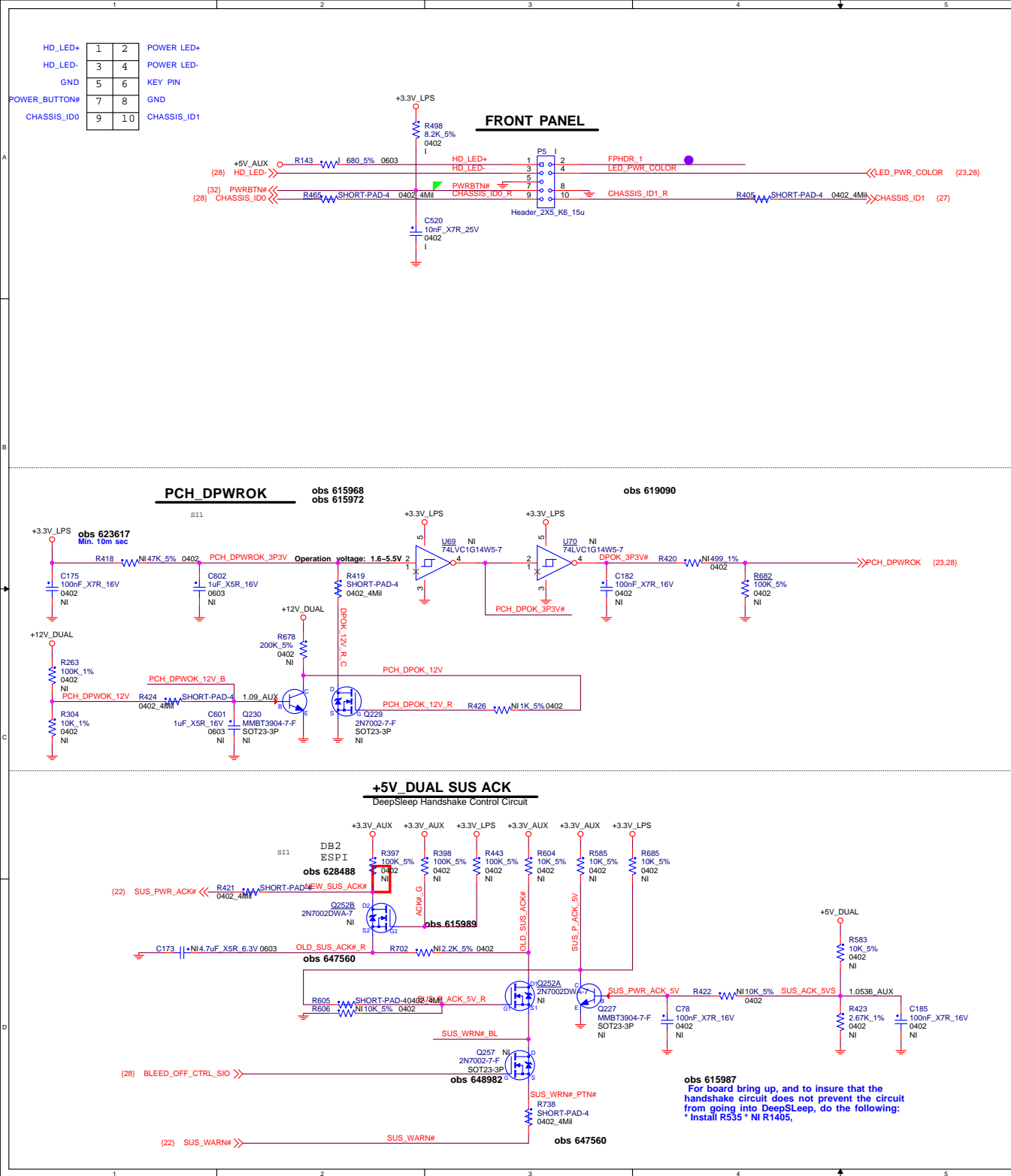
FRONT AUDIO HEADER

PORT_C FOR FRONT MIC_IN

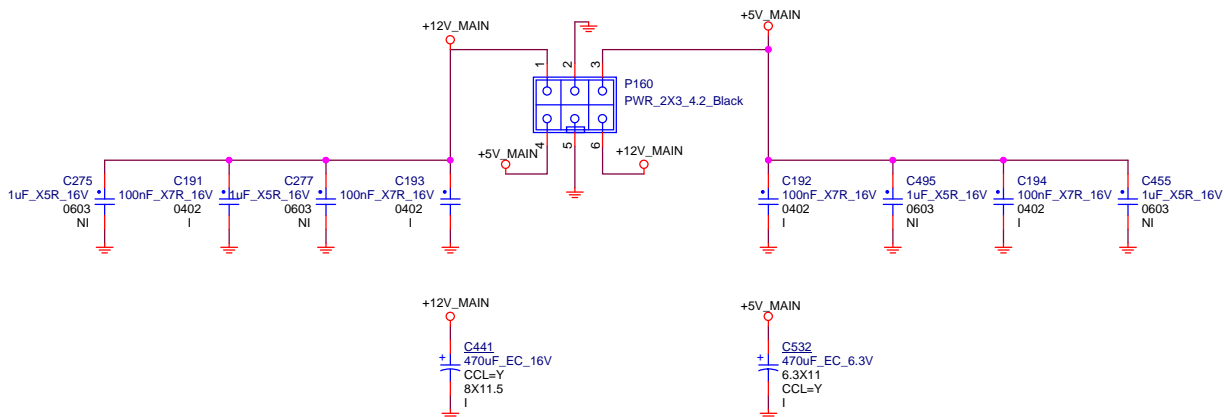
PORT_I FOR FRONT HP_OUT

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Title AUDIO SPEAKER OUT					
Size	Document Number				Rev
Custom	795207-000				A
Date:	Monday, June 29, 2015	Sheet	31	of	72



SATA POWER



PCB1

Printed Circuit Board

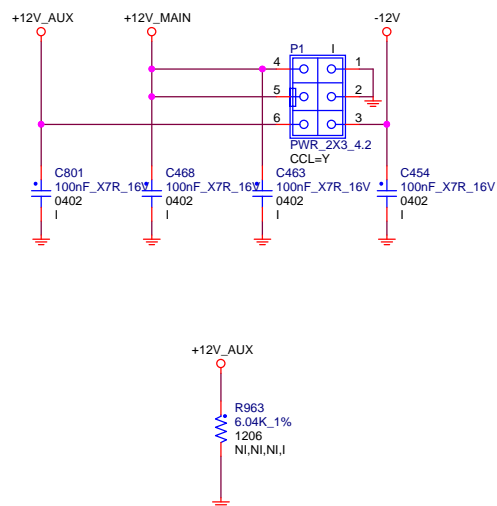
D800 PCB

PCB_REV:A

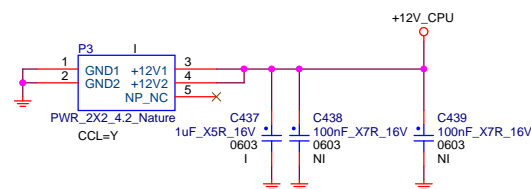
CCL=Y

4-Layer PCB, Color With Green Soldermask, White Silkscreen, NPG-TL, ML1, 9.6X9.6 inch, Rev:A, ROHS, HF
0101AQH08-35K-H

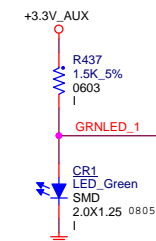
12V Power Connector




VR12V Power Input Connector



+3V_AUX LED

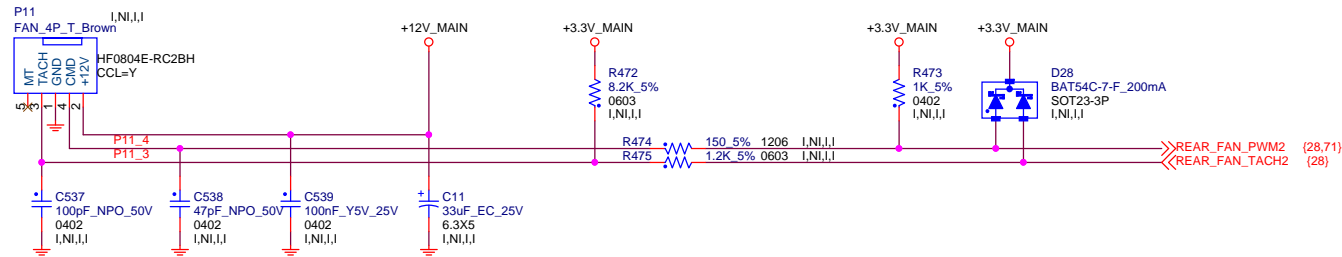


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Title PWR CON/AUXLED/PCB					
Size	Document Number				Rev
Custom	795207-000				A
Date: Wednesday, July 01, 2015		Sheet	35	of	72

Rear Chasis FAN

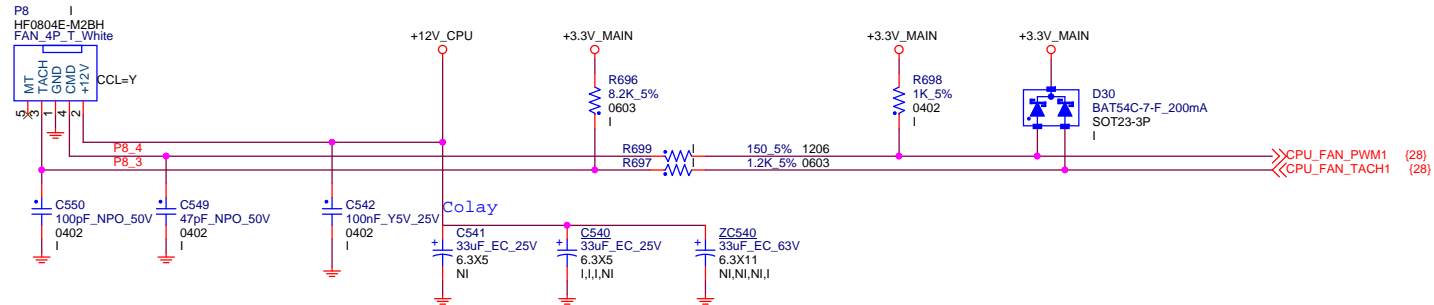
Color: Red



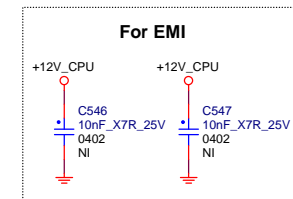
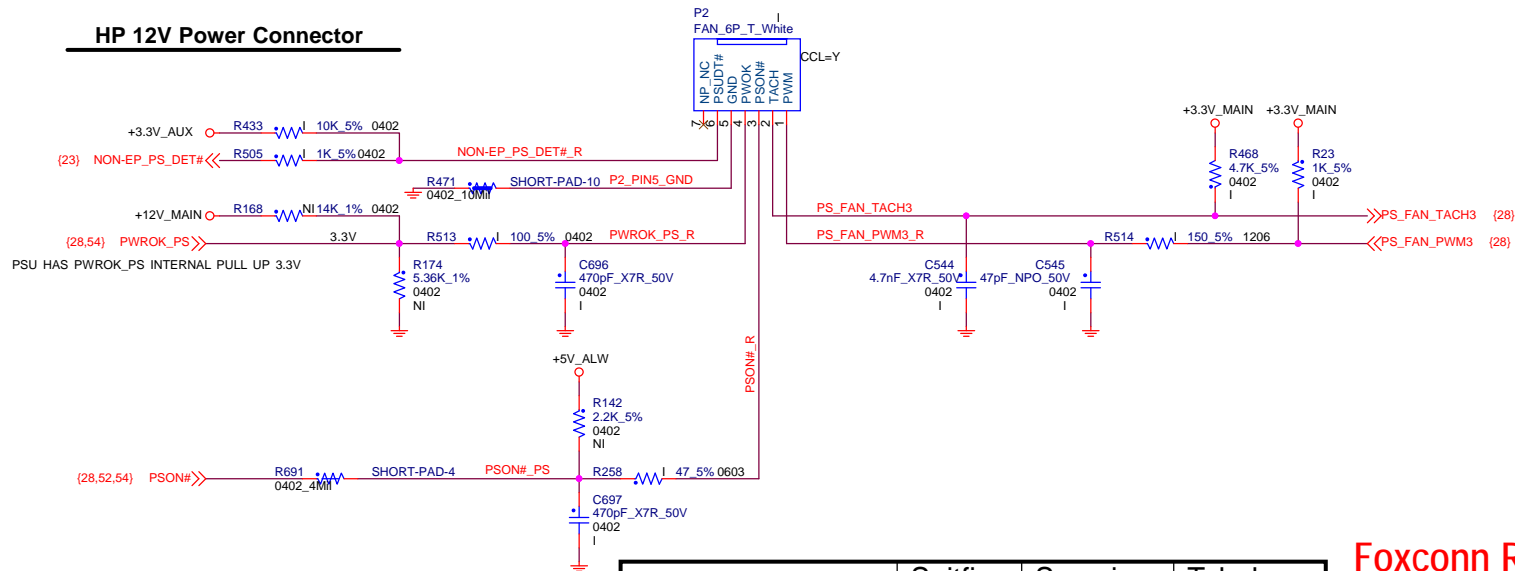
CPU FAN

Color: White

X3



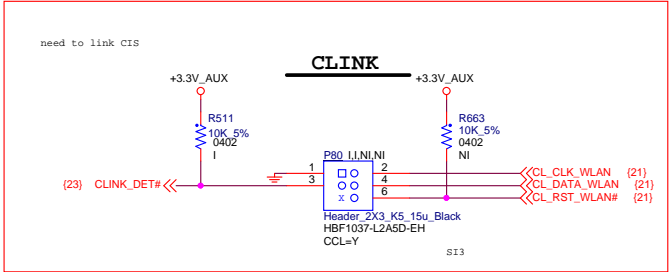
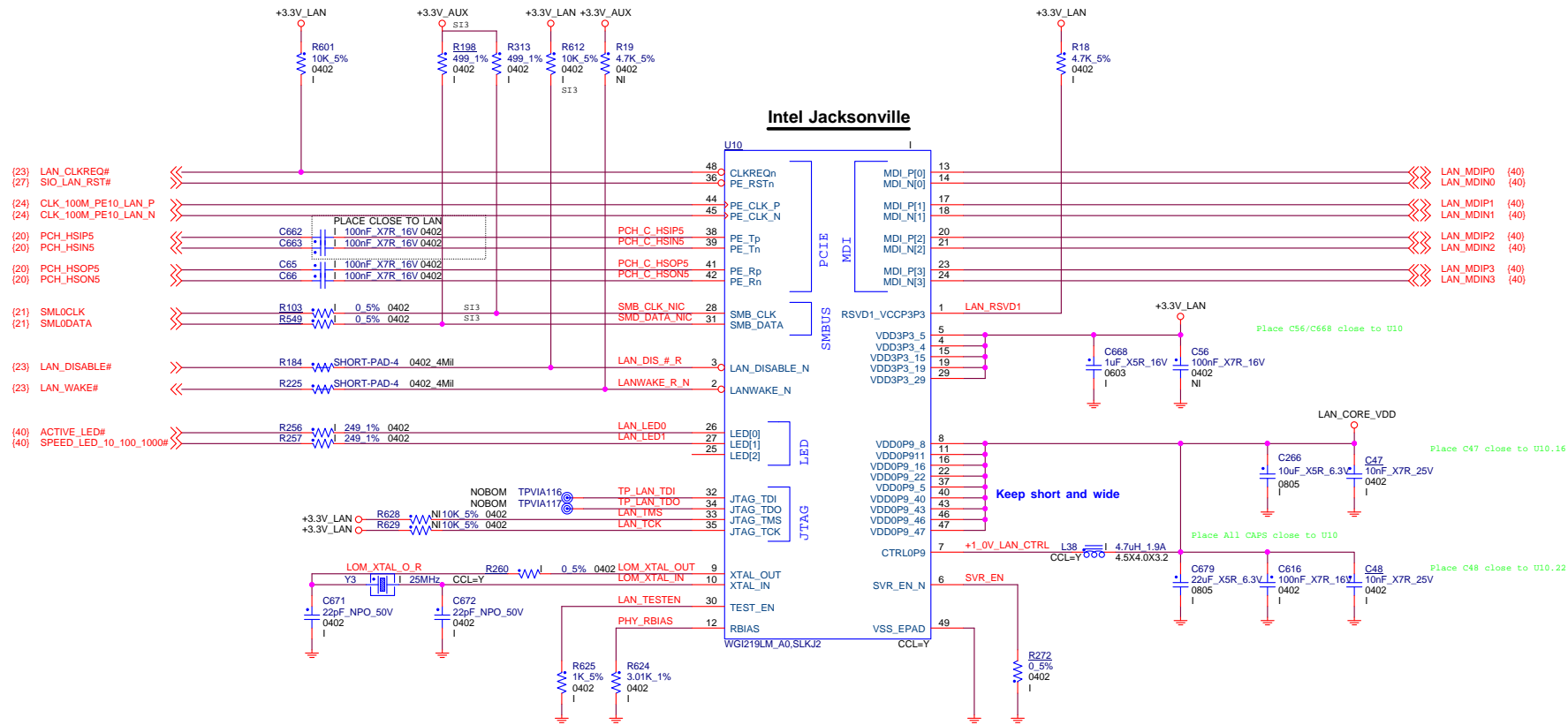
HP 12V Power Connector



	Spitfire	Scorpion	Toledo
CPU FAN - P8	1	1	1
Front FAN - P9	--	--	--
Rear FAN - P11	1	1	--
PSU FAN - P2	1	1	1

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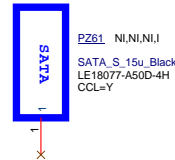
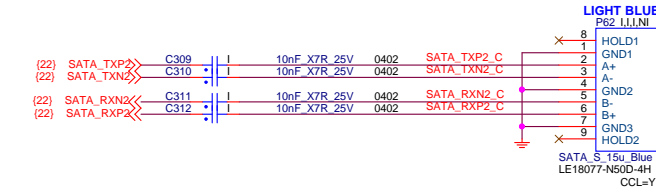
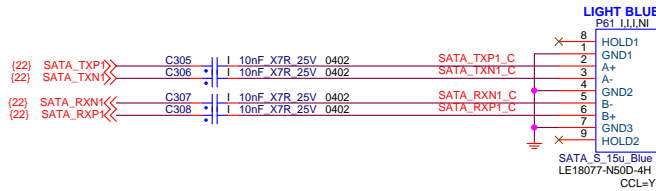
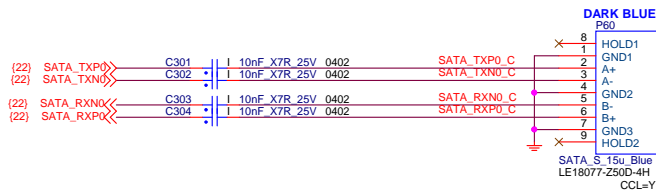
Title: **Intel Jacksonville**

Size: Document Number
Custom: 795207-000

Date: Monday, June 29, 2015

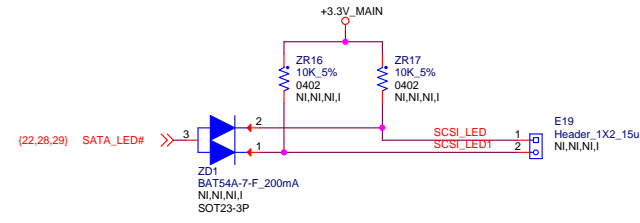
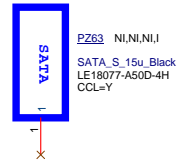
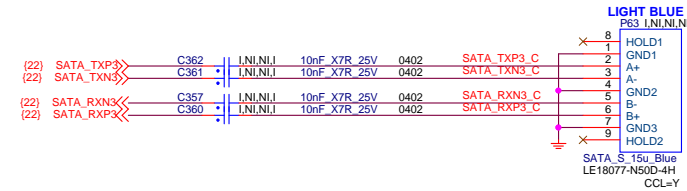
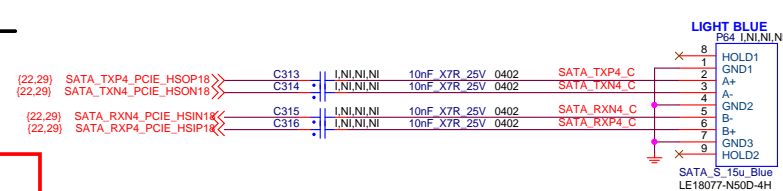
Sheet: 37 of 72

Rev: **A**



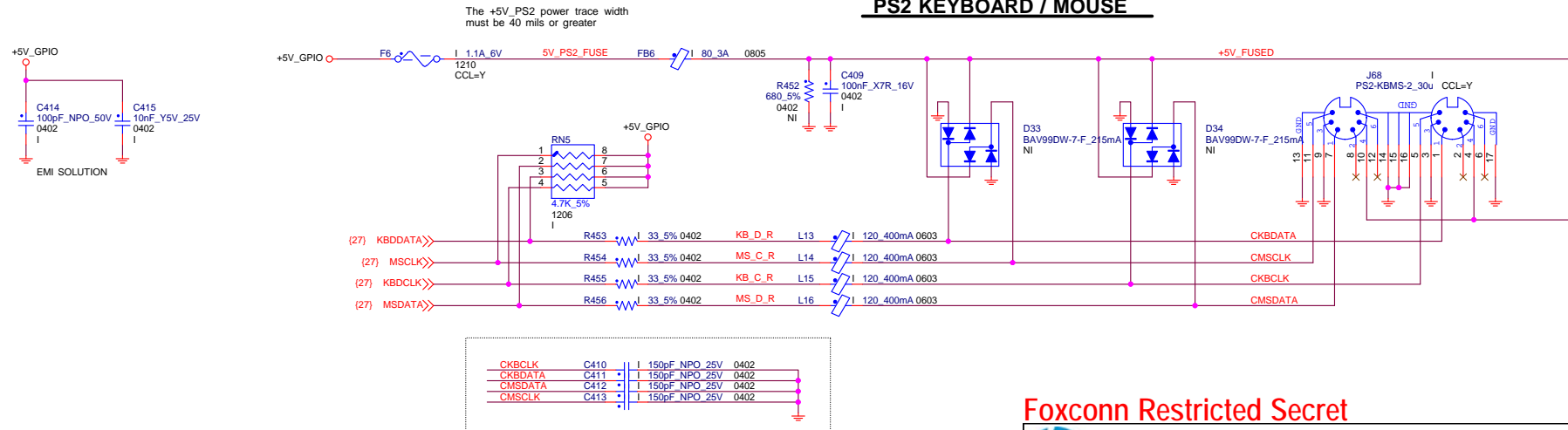
SATA

Spitfire = 5 ports
Scorpion = 3 ports
Toledo = 3 ports
Bunun = 4 ports
PCA spec doesn't define the gold plating.

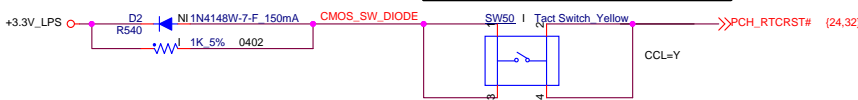


BOM DISTRIBUTION RULE
Spitfire, Scorpion, Toledo, Z2
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PS2 KEYBOARD / MOUSE



CLEAR CMOS BUTTON



CAD NOTE:
The PCB must have this silkscreen for HPQ
This circuit disables the clear CMOS function when system is powered



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Title: SATA/PS2/CMOS

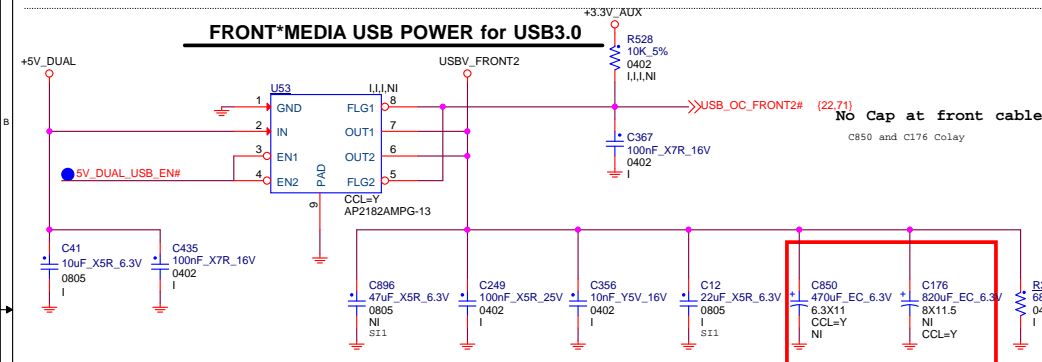
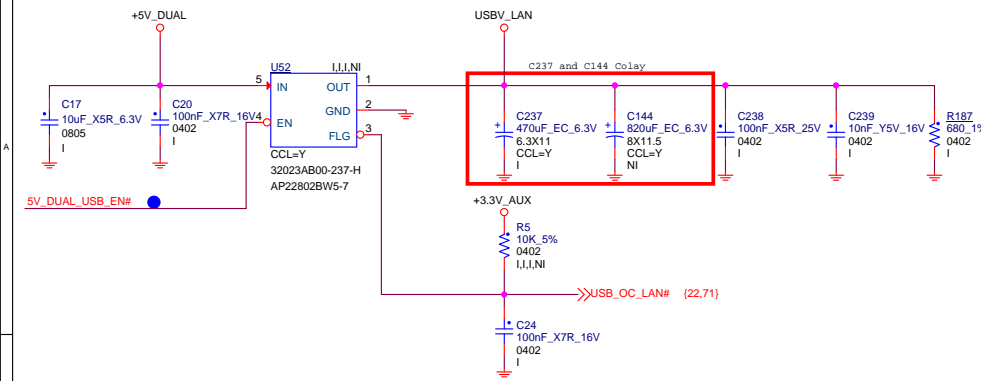
Size: Document Number
Custom: 795207-000

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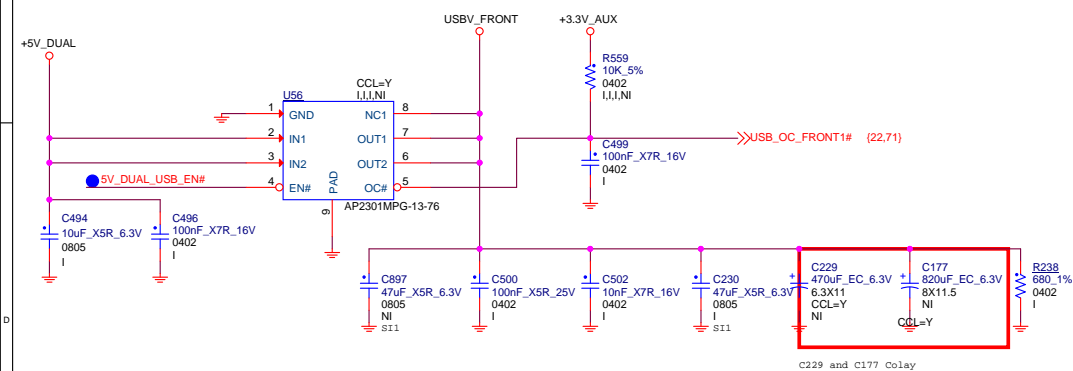
LAN+USB3x2



Have to check 2nd source's footprint and symbol

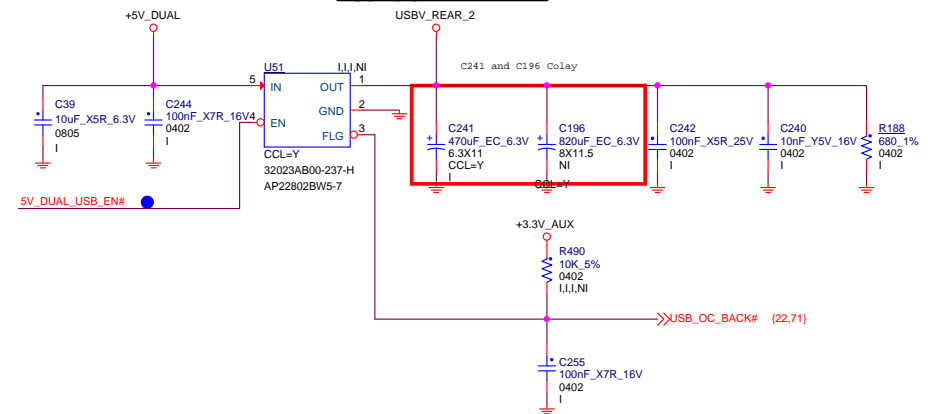
Combine the Front and Media power rail by one power switch topology. 1.5A/1CH - Dual CH

FRONT USB POWER for USB2.0



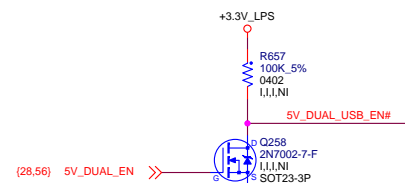
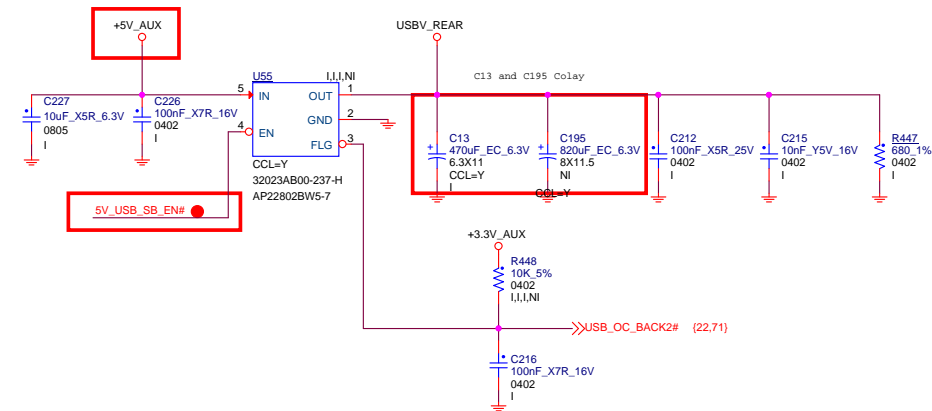
Have to check 2nd source's footprint and symbol

REAR USB POWER USB3.0x2



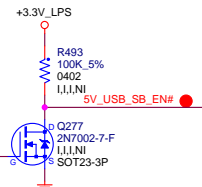
Wake-up event by USB device at S0-S5 state
2*USB3 Port
+5V_AUX + GPIO control

REAR USB POWER USB3.0x2



GPIO Power Well = DSW
or SUS
Need to use SIO GPIO

GPIO	5V_USB_SB_EN#
H	Switch On
L	Switch Off

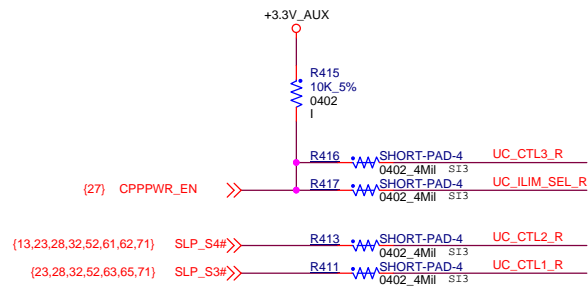
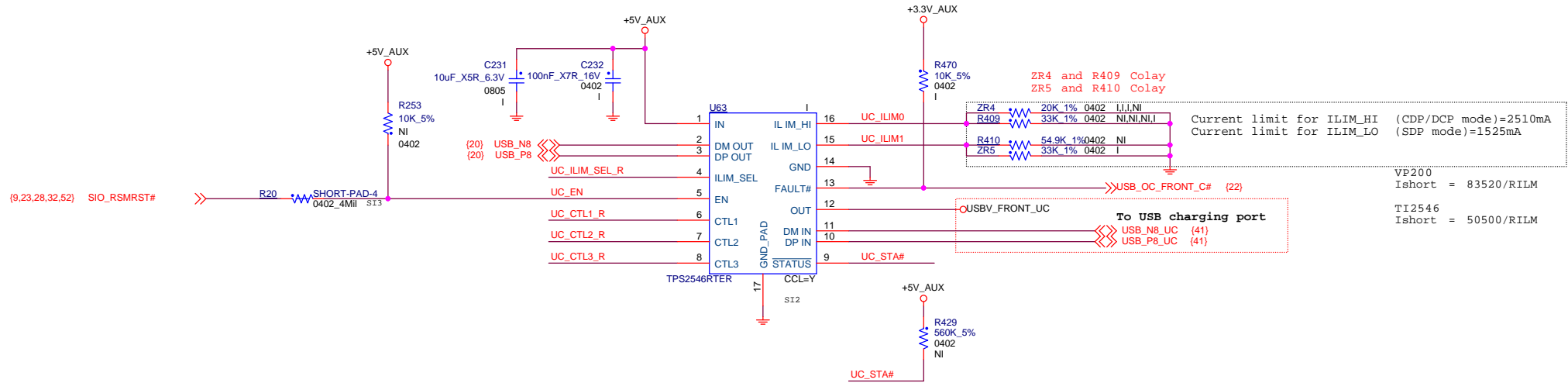


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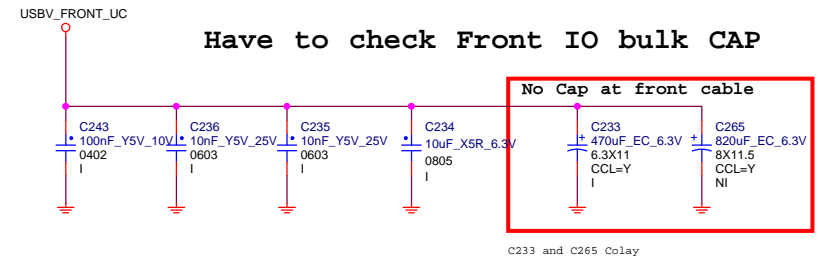
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USB CHARGER



PCH GPIO41 for PCH_CHAR_CTL3
(H-->CDP, L-->SDP)



USB Charging mode selection in System Status

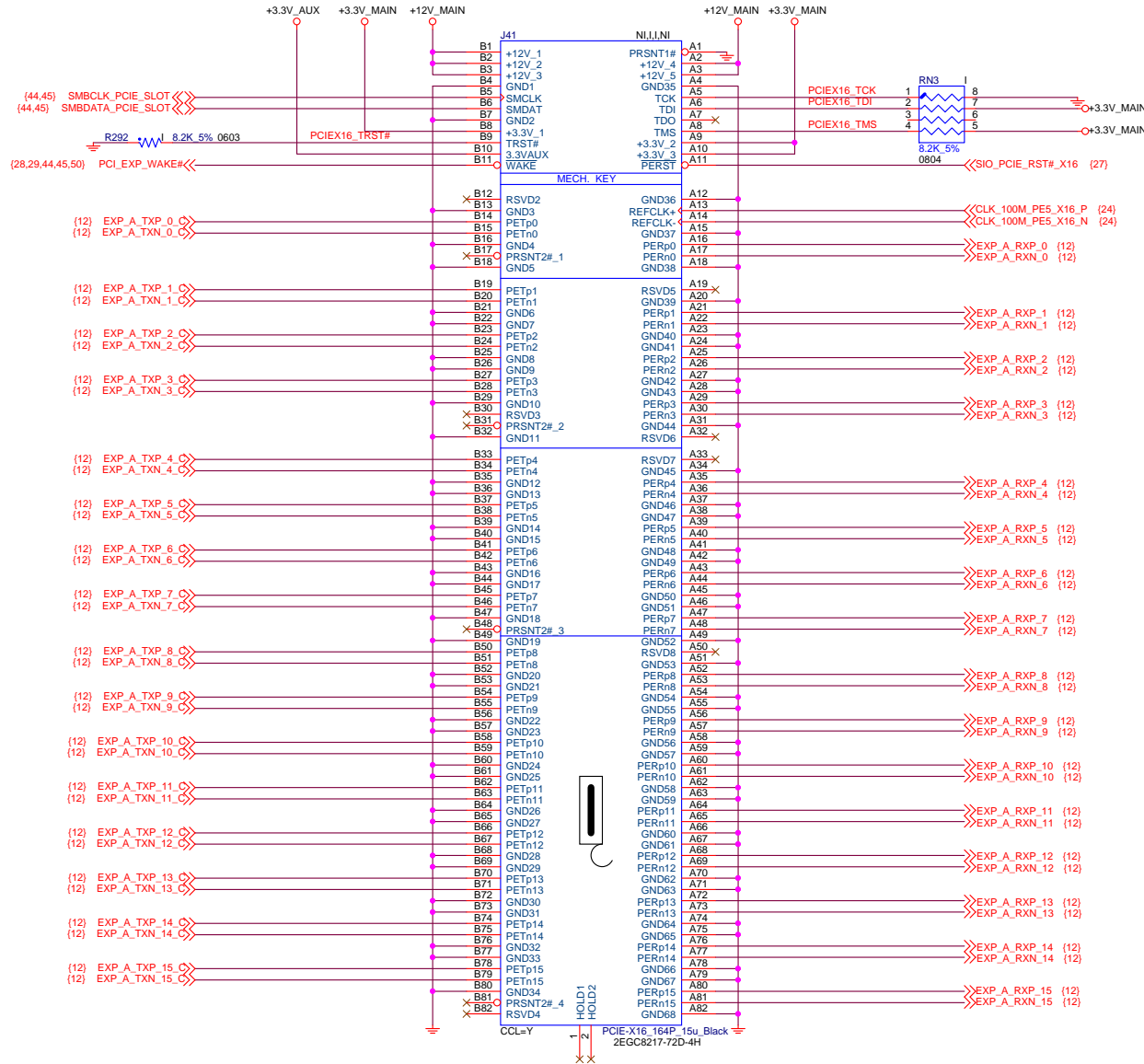
State	bit	CTL1 SLP_S3#	CTL2 SLP_S4#	CTL3 CPPPWR_EN	ILIM_SEL	Mode	ILIM
S0		1	1	1	1	CDP	ILIM = 2510mA
S0		1	1	0	0	SDP	ILIM = 1525mA
S3		0	1	1	1	DCP_AUTO	ILIM = 2510mA
S3		0	1	0	0	SDP	ILIM = 1525mA
S4/S5		0	0	1	1	DCP	ILIM = 2510mA
S4/S5		0	0	0	0	TURN OFF SWITCH	ILIM = 1525mA

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Title USB CHARGER					
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PCI EXPRESS x16 SLOT



Need to change to 15u" for ENT
2EG78217-72DL-4H

JS41

I,NI,NI,NI

JZ41

NI,NI,NI,I

Spitfire PCIE-X16_15u" CLIP 15u" Bunun PCIE-X16_30u" colay with J41

PCIE-X16, 164P, 15u
2EG78217-72DL-4H
CCL=Y
34030GT00-600-H

PCIE-X16, 164P, 30u
2EG08213-72D-DH
CCL=Y

+3.3V_AUX



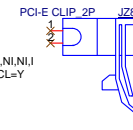
+3.3V_MAIN



+12V_MAIN



Colay

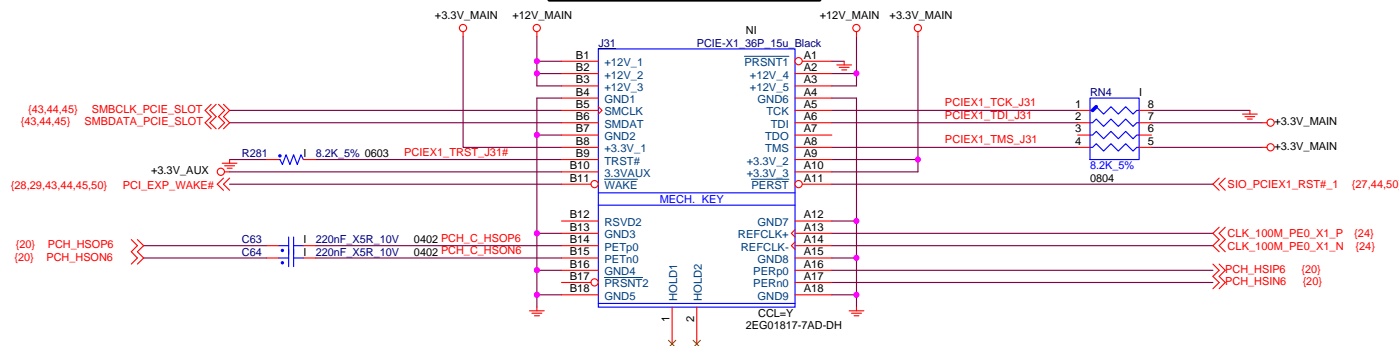


Z2 leverage change item

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Date:	Monday, June 29, 2015	Sheet	43 of 72

PCI EXPRESS X1 SLOT1



JS31 I,I,I,NI

Toledo PCIE-X1_15u"
colay with J31

PCIE-X1_36P_15u_Black
2EG01817-7ADR-DH

JS32 I,I,I,NI

Toledo PCIE-X1_15u"
colay with J32

PCIE-X1_36P_15u_Black
2EG01817-7ADR-DH

JZ31 NI,NI,NI,I

Bunun PCIE-X1_30u"
colay with J31

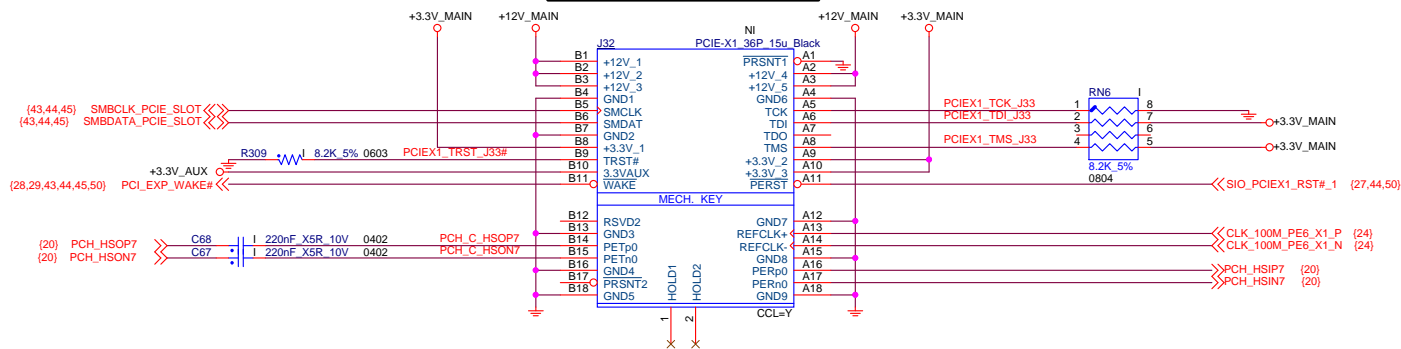
PCIE-X1_36P_30u
AAA-PCI-003-W82
CCL=Y

JZ32 NI,NI,NI,I

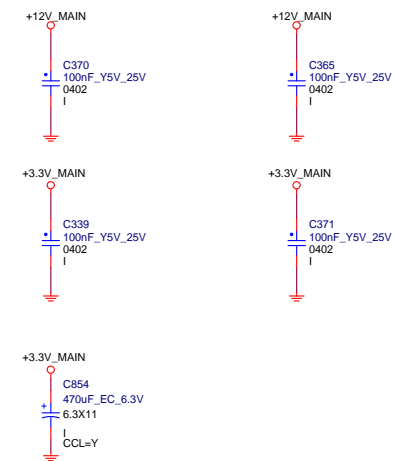
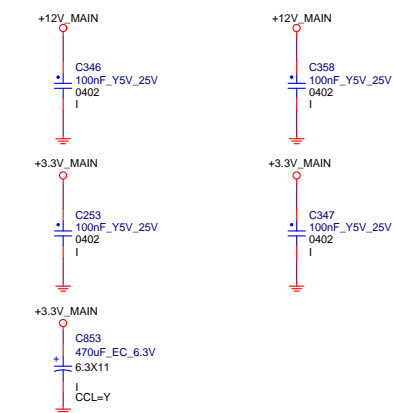
Bunun PCIE-X1_30u"
colay with J32

PCIE-X1_36P_30u
AAA-PCI-003-W82
CCL=Y

PCI EXPRESS X1 SLOT1



	SIO_GPIO25	SIO_GP60 / CLAMP_CTRL	+3_3V_SLOT
S0	X	L	ENABLE
S3 / S5	H	H	ENABLE
WOL DISABLE	L	H	DISABLE



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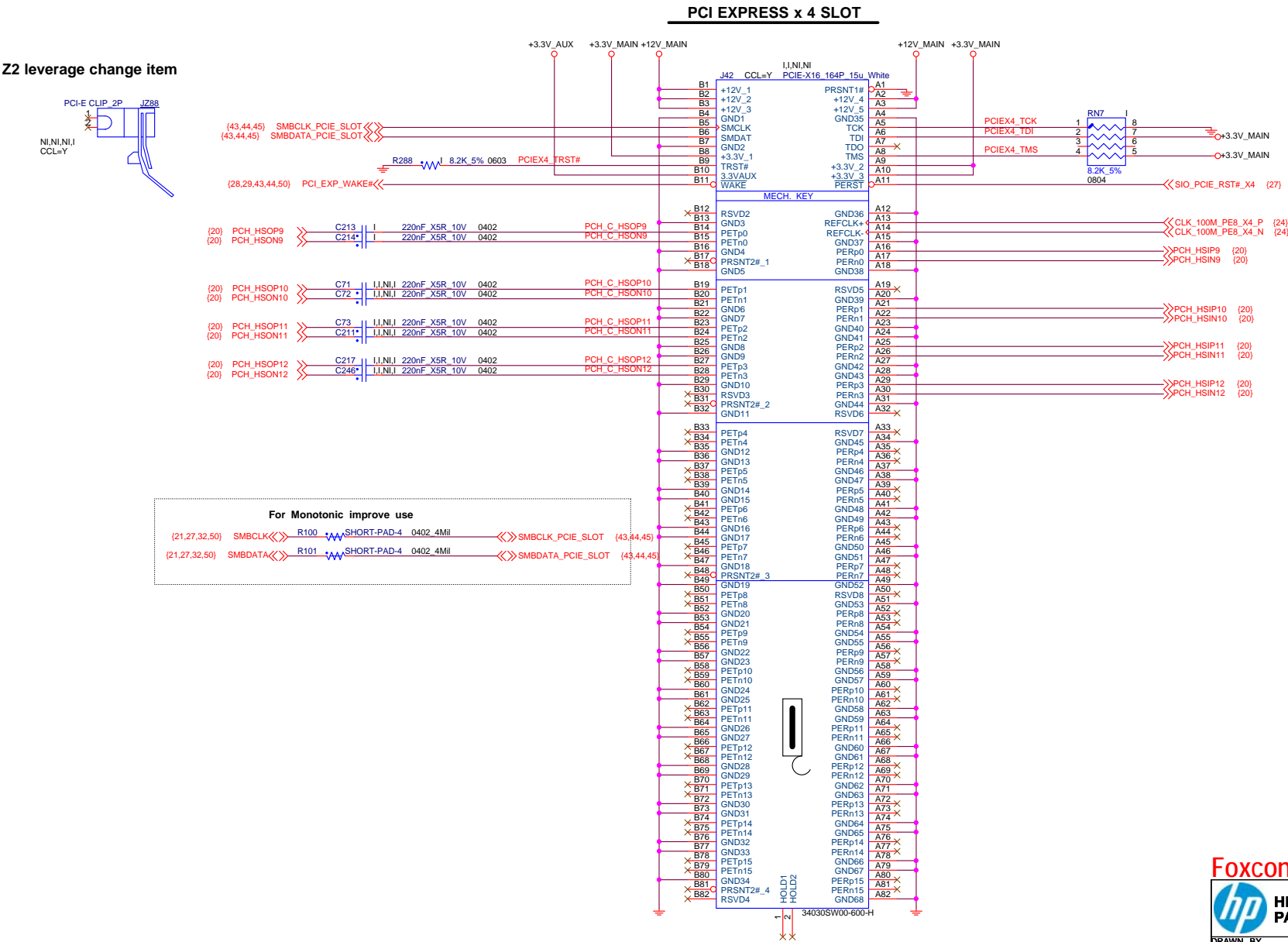
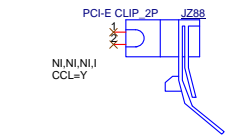
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Sheet 44 of 72
 Rev **A**

Z2 leverage change item

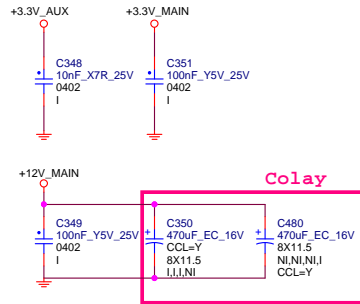


JS42 NI,NI,NI,NI
Toledo PCIE-X1_15u" colay with J42

PCIE-X1_36P_15u_Black
2EG01817-7ADR-DH

JZ42 NI,NI,NI,NI
Bunun PCIE-X16_30u" colay with J42

PCIE-X16_164P_30u
2EG08213-72D-DH
CCL=Y

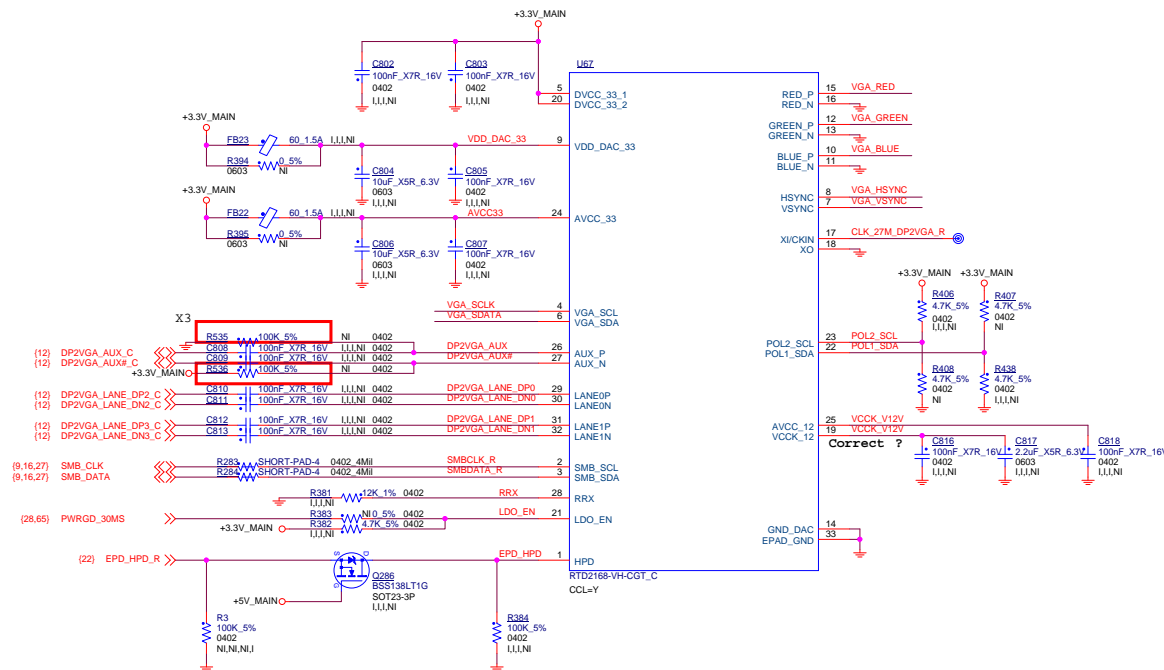


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Spitfire, Scorpion, Toledo, Z2
(BOM,BOM,BOM, BOM)

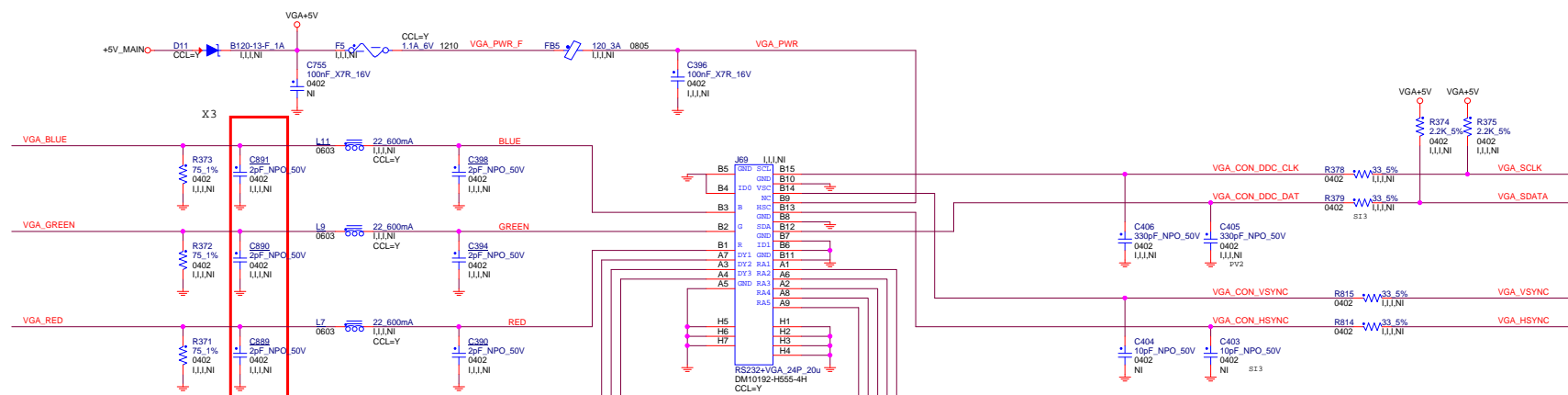
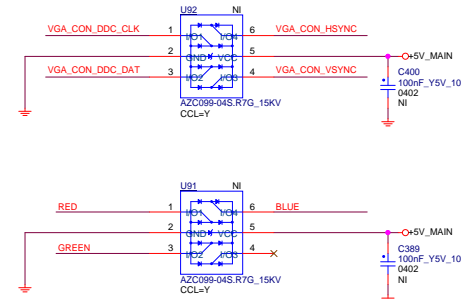
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DP to VGA_RTD2168



ESD pads are as close as possible to I/O connector pins. capacitor pads are as close as possible to the ESD diode.



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Spitfire, Scorpion, Toledo, Z2
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Document Number

Size	Document Number
C	795207-000

Date: Monday, June 29, 2010

Rev
A

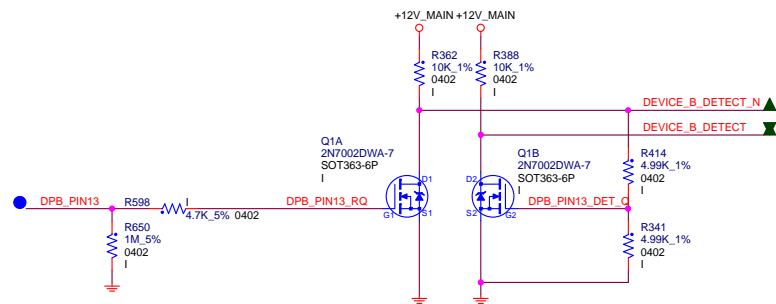
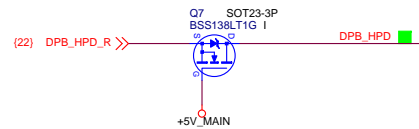
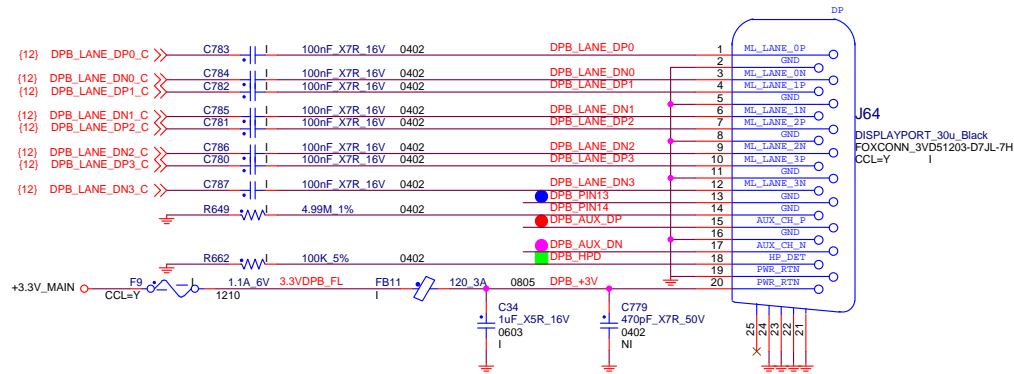
Sheet 46 of 72

	Sheet	48	51	72
			8	

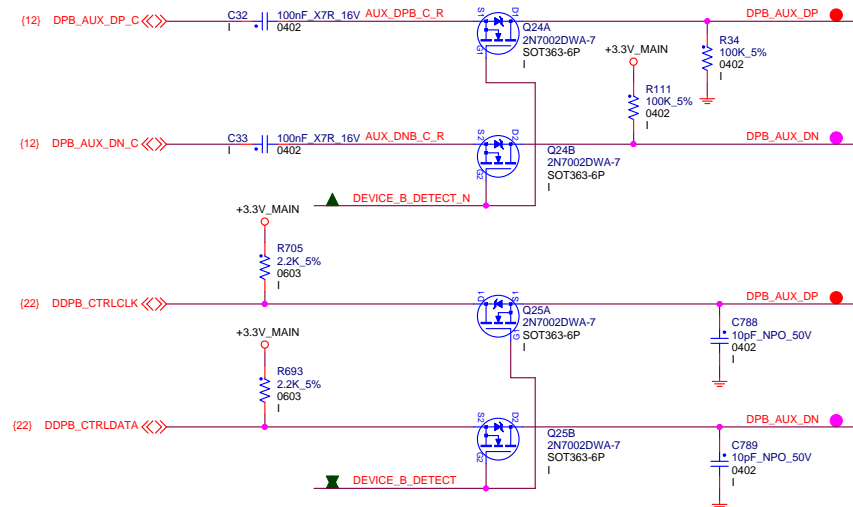
Bunun COM PORT ONLY
colay with J69

RS232_9P_20u_Teal
DM10192-H543-4H
CCL=Y

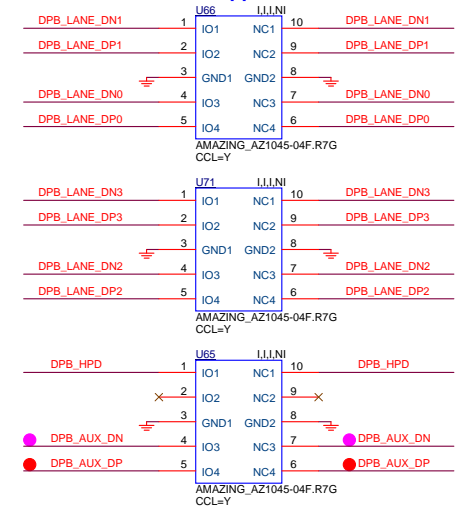
DISPLAY PORT



PIN13		FUNCTION
DP	DONGLE	
L	X	DEVICE_C_DETECT
X	H	DEVICE_C_DETECT_N



ESD suppressor



Bunun DP ESD



Bunun DP ESD



Bunun DP ESD



BOM DISTRIBUTION RULE
Spitfire, Scorpion, Toledo, Mondial
(BOM,BOM,BOM, BOM)

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Title	DISPLAY PORT 1(SINGLE)
-------	------------------------

Size	Document Number
Custom	795207-000

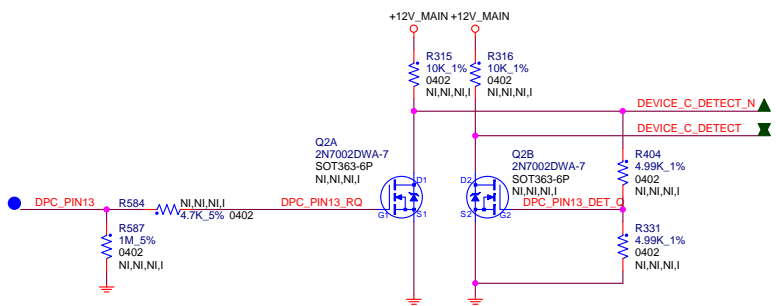
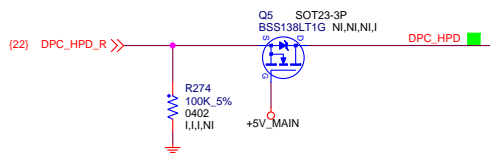
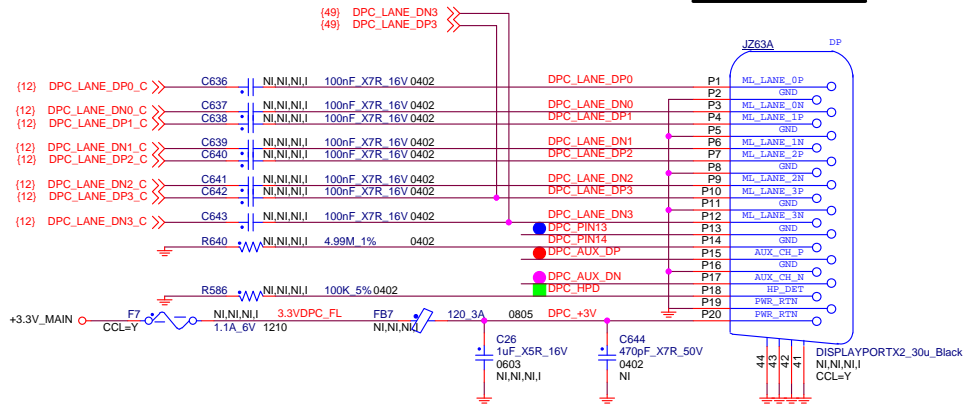
Date: Monday, June 29, 2015

Rev
A

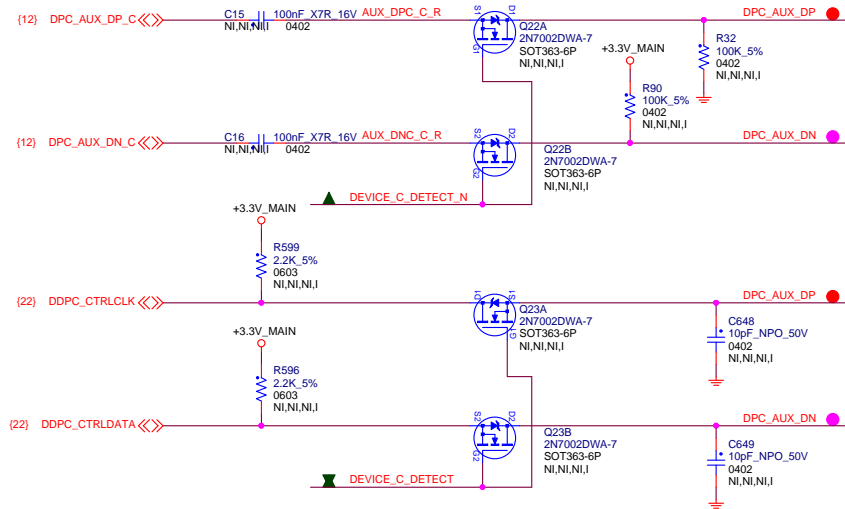
Date: Monday, June 29, 2015

Sheet 47 of 72

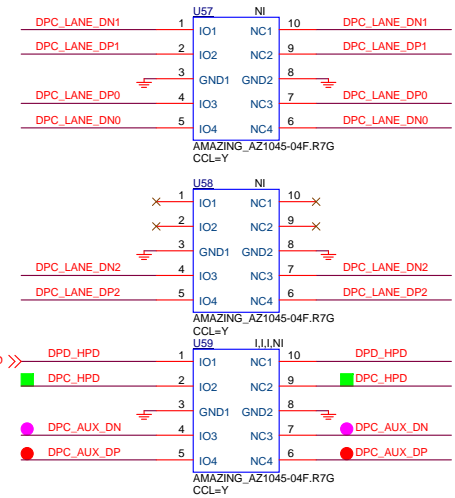
WKS Only
DISPLAY PORT



PIN13		FUNCTION
DP	DONGLE	
L	X	DEVICE_C_DETECT
X	H	DEVICE_C_DETECT_N



ESD suppressor



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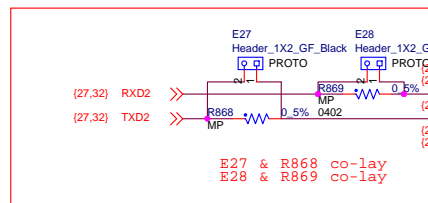
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Title	DISPLAY PORT 2(DUAL-C)
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Size	Document Number
Custom	795307-000

Date: Monday, June 29, 2015

Rev
A

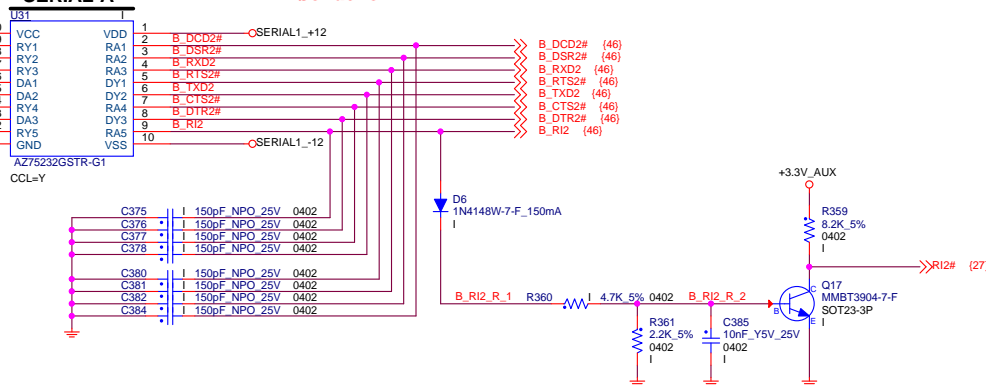


@E27(1-2)
Jumper_2P_GF_Blue
PROTO

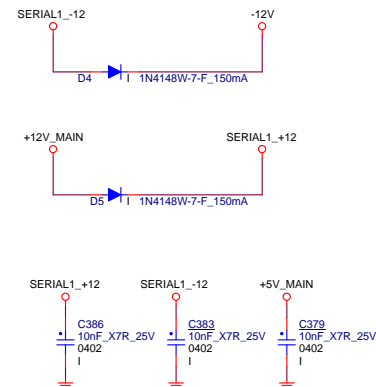
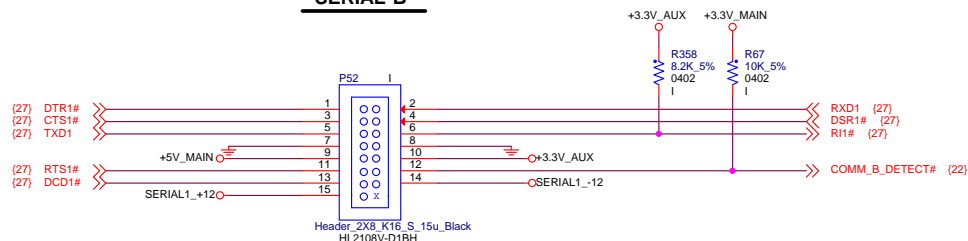
@E28(1-2)
Jumper_2P_GF_Blue
PROTO

SERIAL A

12V solution



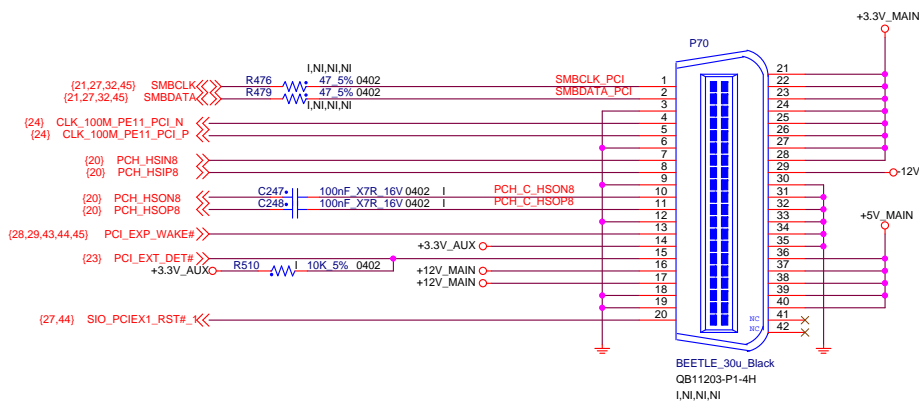
SERIAL B



Serial B

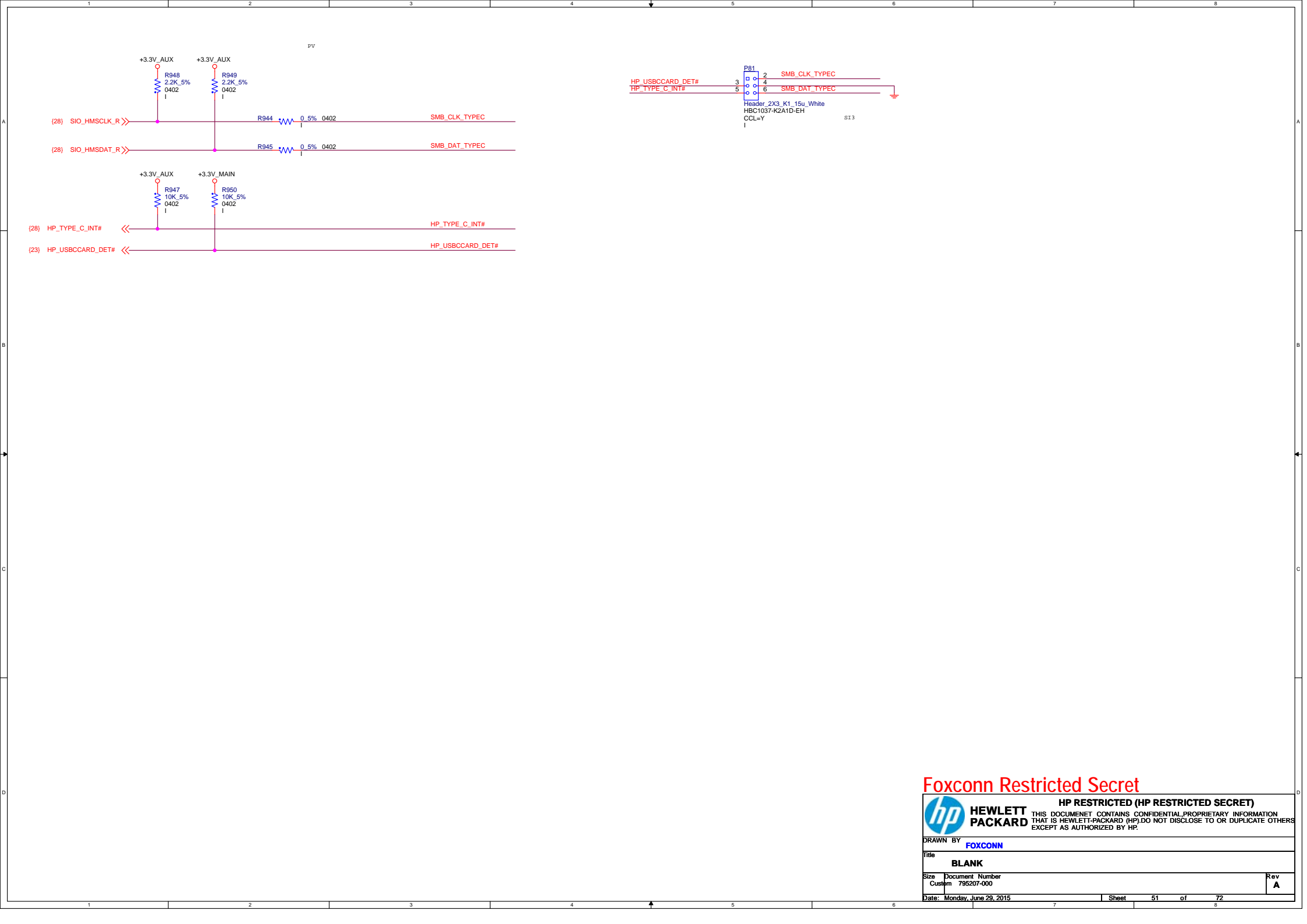
1 COM_DTR1#	2 COM_SDIN1
3 COM_CTS1#	4 COM_DSR1#
5 COM_SDO1	6 COM_RI1#
7 GND	8 GND
9 +5V_SYS	10 +3.3V_SB
11 COM_RTS1#	12 COM_DET#
13 COM_DCD1#	14 -12V_SYS
15 +12V_SYS	16 KEY

SCSI Connector




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Title COMA/COMB/SCSI			
Size	Document Number	Rev A	
Custom	795207-000		
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Title
BLANK

Size
Custom

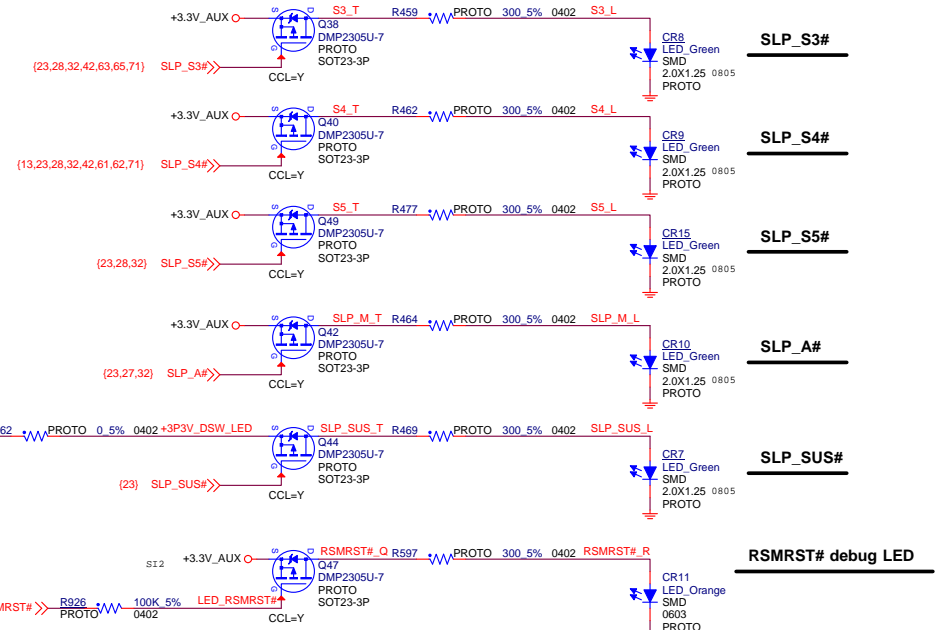
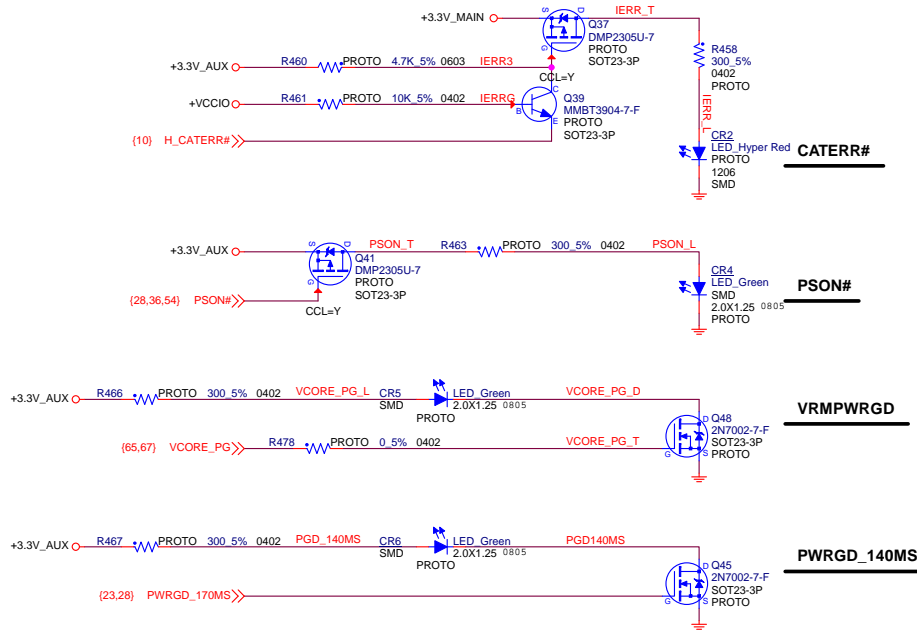
Document Number
795207-000

Date: Monday, June 29, 2015

Rev
A

Sheet
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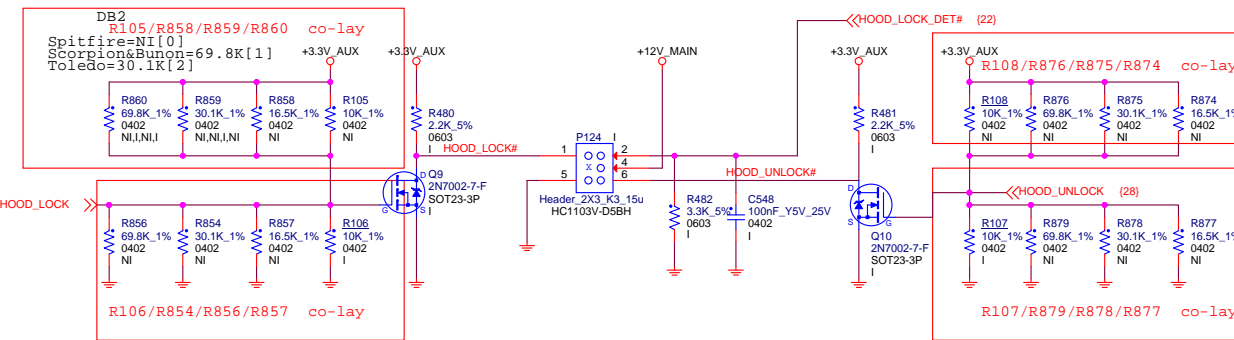
PCA LEDs



R105/R106 control ML_STR1 PCA_ID[2:0]

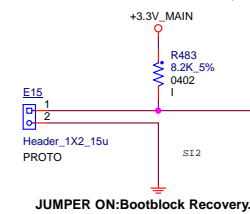
HOOD LOCK CIRCUIT

R108/R107 control ML_STR2 PCA_ID[5:3]



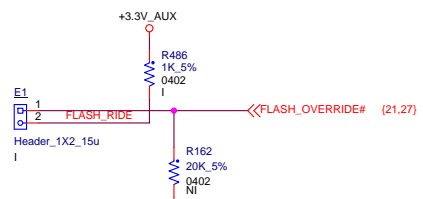
BOOTBLOCK RECOVERY

E15: SPI ROM bootblock recovery header



FLASH OVERRIDE

HDA_SDO: A weak internal pull down. Strap low, the security measures defined in the Flash Descriptor will be in effect (default). Sample high, Flash Descriptor Security will be overridden.



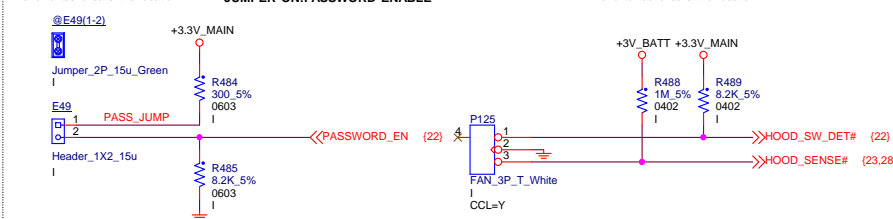
PCA_ID Resistor values

PCA Assignments	PCA_ID	ML_STR2 pin	ML_STR1 pin
SPITFIRE	0	NI	10K
SCORPION/BUNUN	1	NI	10K
TOLEDO	2	NI	10K
	3	NI	10K
	4	NI	10K
	5	NI	10K
	6	NI	10K
	7	NI	10K

PASSWORD JUMPER

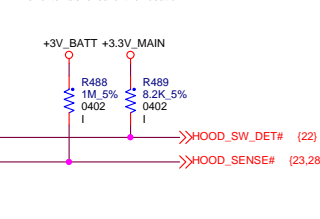
Have to take care the location

JUMPER ON:PASSWORD ENABLE



HOOD SENSE CIRCUIT

Have to take care the location

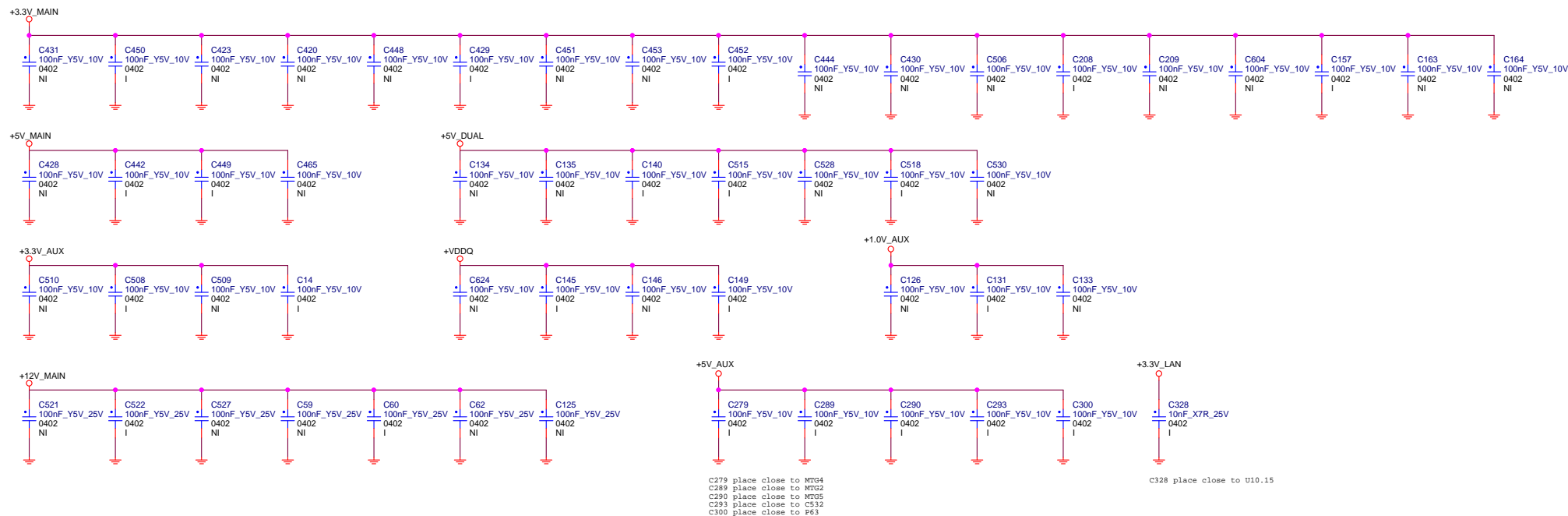


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(BOM,BOM,BOM, BOM)

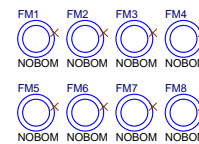
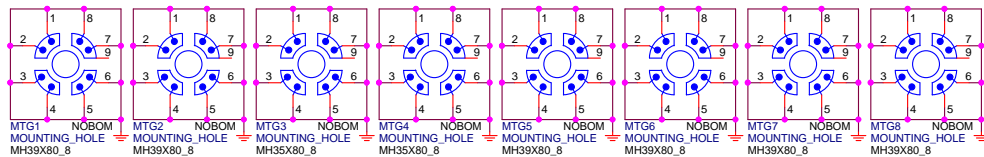
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EMI CAP



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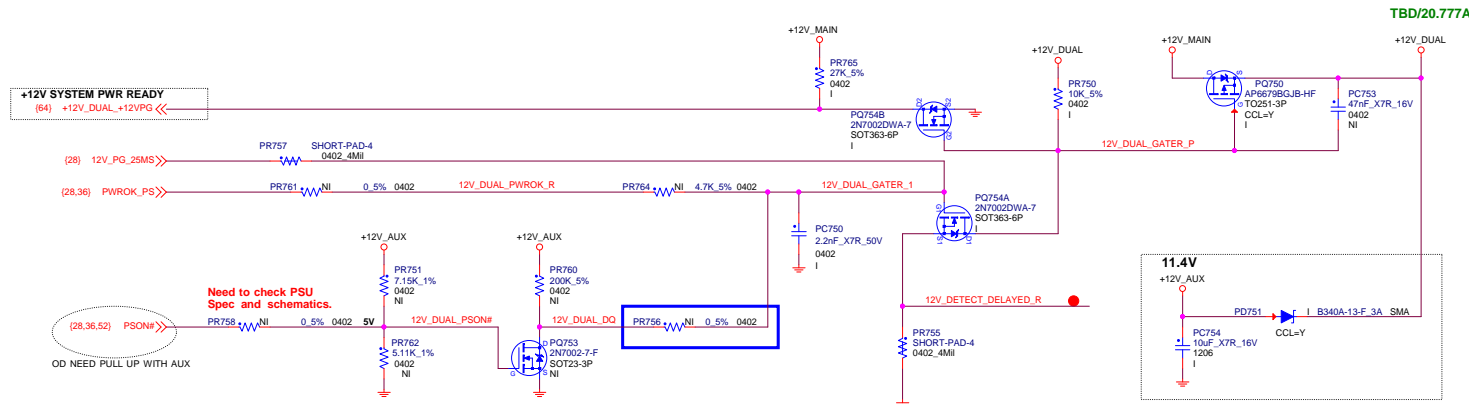


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Title		FEATRUES			
Size	Document Number			Rev	
Custom	795207-000			A	
Date: Monday, June 29, 2015		Sheet		53	of 72

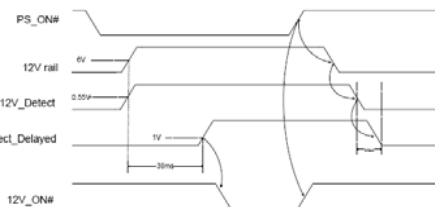
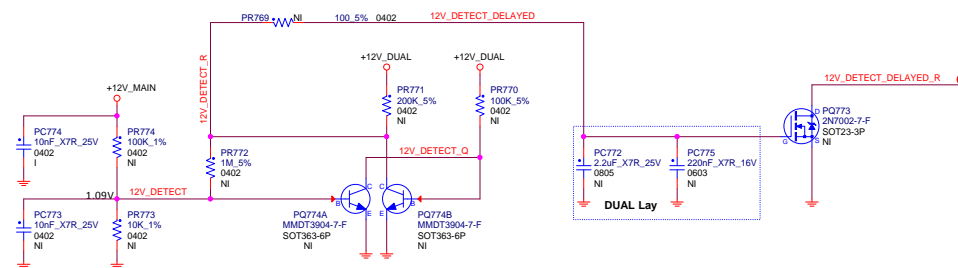
Note: net-name:12V

+12V_DUAL



12V DETECT DELAY CIRCUIT

PROTO PARTS



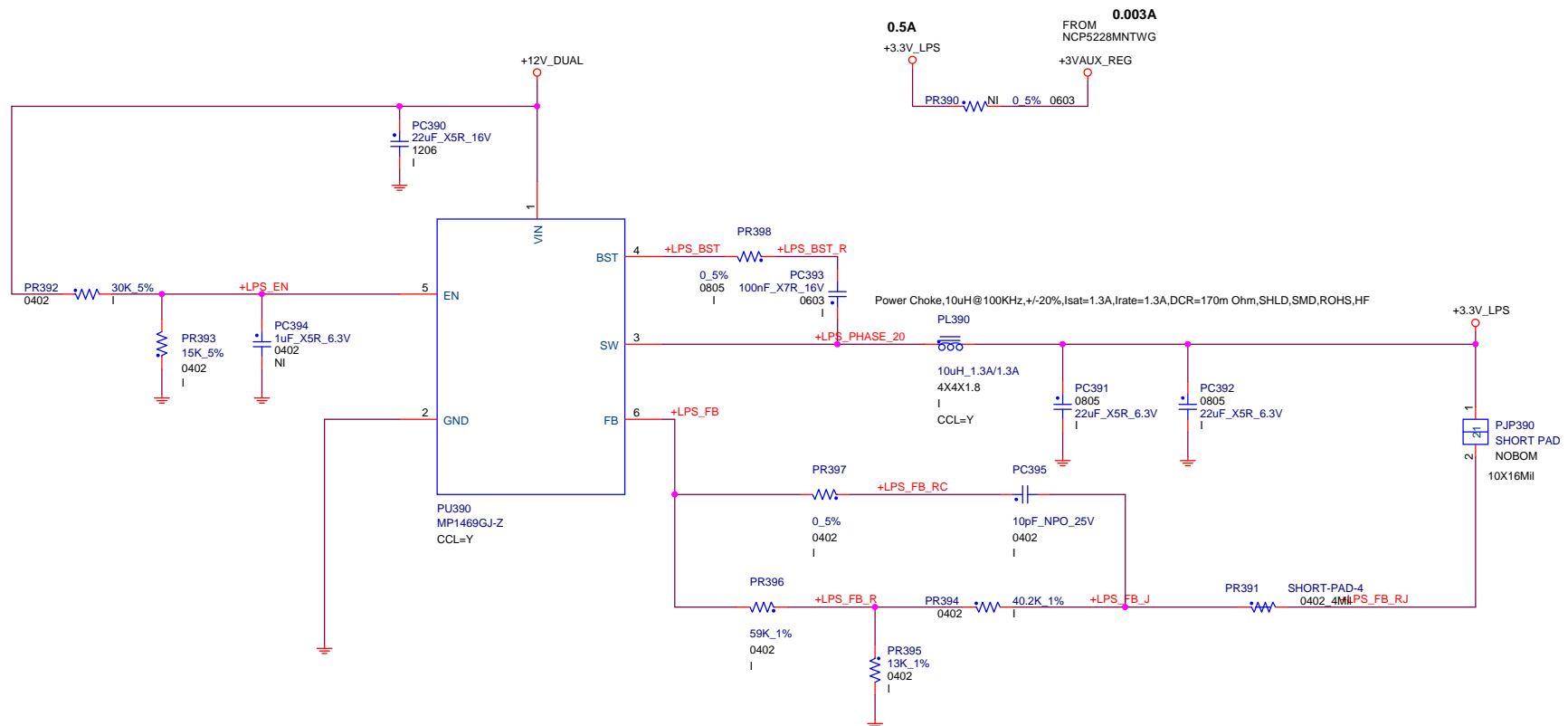
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DRAWN BY: FOXCONN	
File: +12V_DUAL	
Size: C	Document Number: A
Date: Monday, June 29, 2015	Sheet: 54 of 72


+3P3V LPS

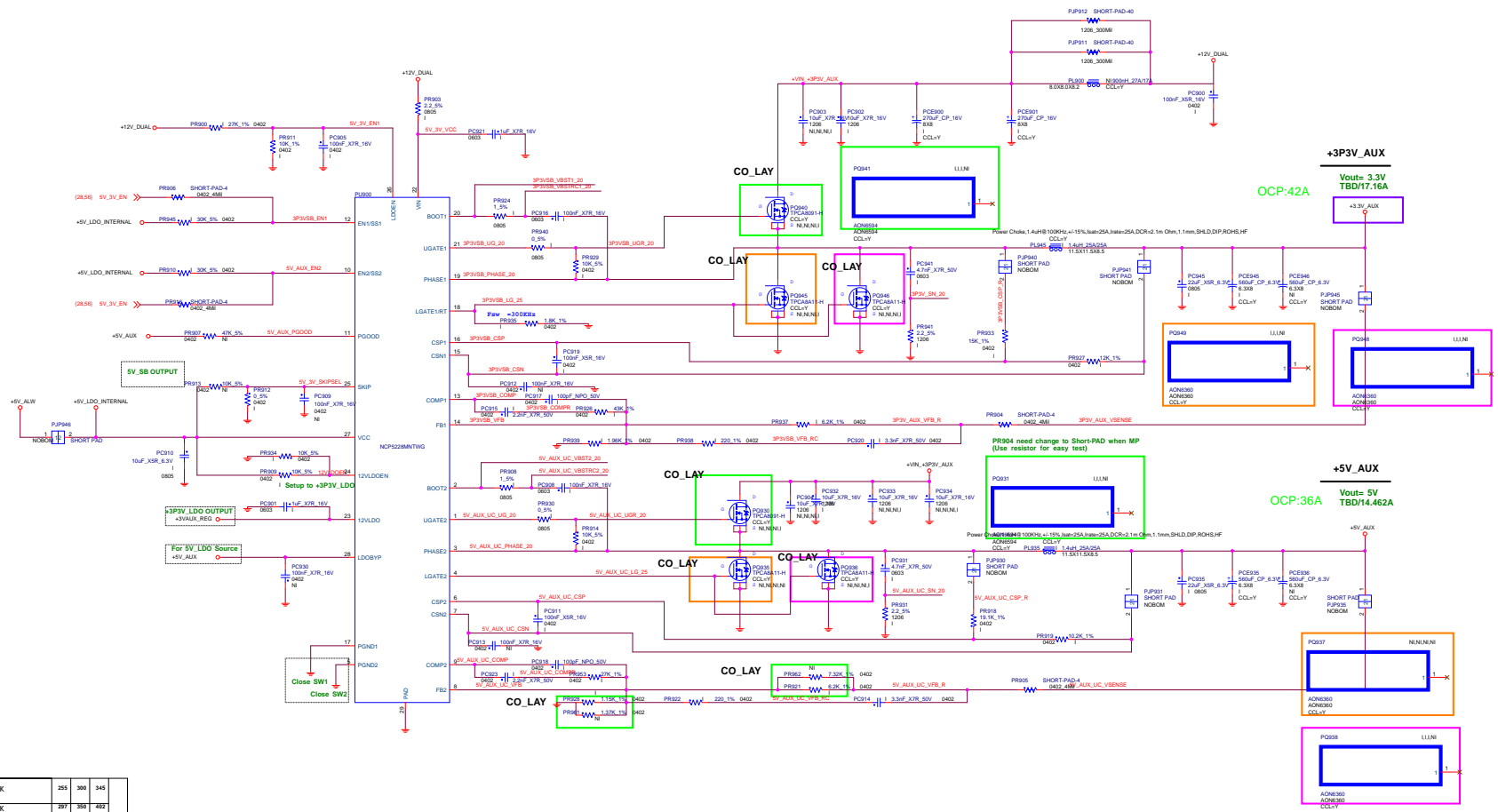
+3P3V_STBY_DSW

Vout= 3.3V
TBD/0.00206A
SO 0.502A



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DRAWN BY FOXCONN					
Title +3P3V_LPS					
Size Custort	Document Number 795207-000				Rev A
Date:	Monday, June 29, 2015		Sheet	55 of 72	



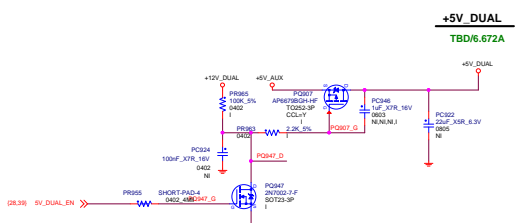
Switching Frequency	f _{sw}	RLGS = 1.8K	255	300	345
		RLGS = 4.7K	397	358	402
		RLGS = 9.1K	348	408	460
		RLGS = 14K	319	400	490

RT8122 Truth Table							
LDOEN	1VLDEN	EN1	EN2	1VLD0	Vcc(+5V)	Vout1	Vout2
L	L	X	X	L	L	L	L
L	2.5V/5V	X	X	3.3V/12V	L	L	L
H	L	X	L	L	H	H	L
H	L	L	L	L	H	L	L
H	2.5V/5V	H/L	H/L	3.3V/12V	H	H/L	H/L

NCF5228 Truth Table							
LDOEN	1VLDEN	EN1	EN2	1VLD0	Vcc(+5V)	Vout1	Vout2
L	X	X	X	L	L	L	L
L	2.5V/5V	X	X	L	L	L	L
L	2.5V/5V	H/L	H/L	3.3V/12V	H	H/L	H/L
H	2.5V/5V	H/L	H/L	3.3V/12V	H	H/L	H/L

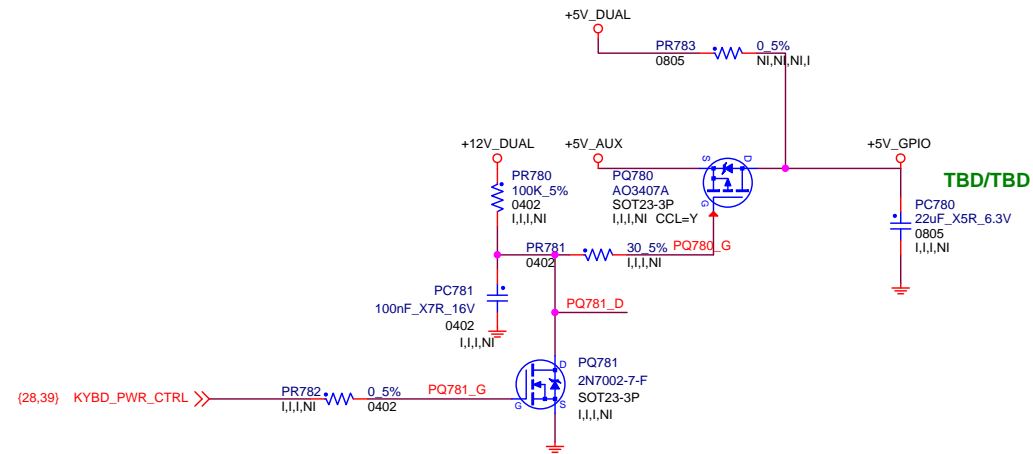
System Power Control Signal Truth Table				
	LPS	S5	S3	S0
5V_3V_EN	L	X	X	X
3P3V5B_EN	L	H	H	H
5V_DUAL_EN	X	L	H	H

System Power State Truth Table				
	LPS	S5	S3	S0
+5V_ALW	H	H	H	H




+3 V_AUX Bleed off Circuit

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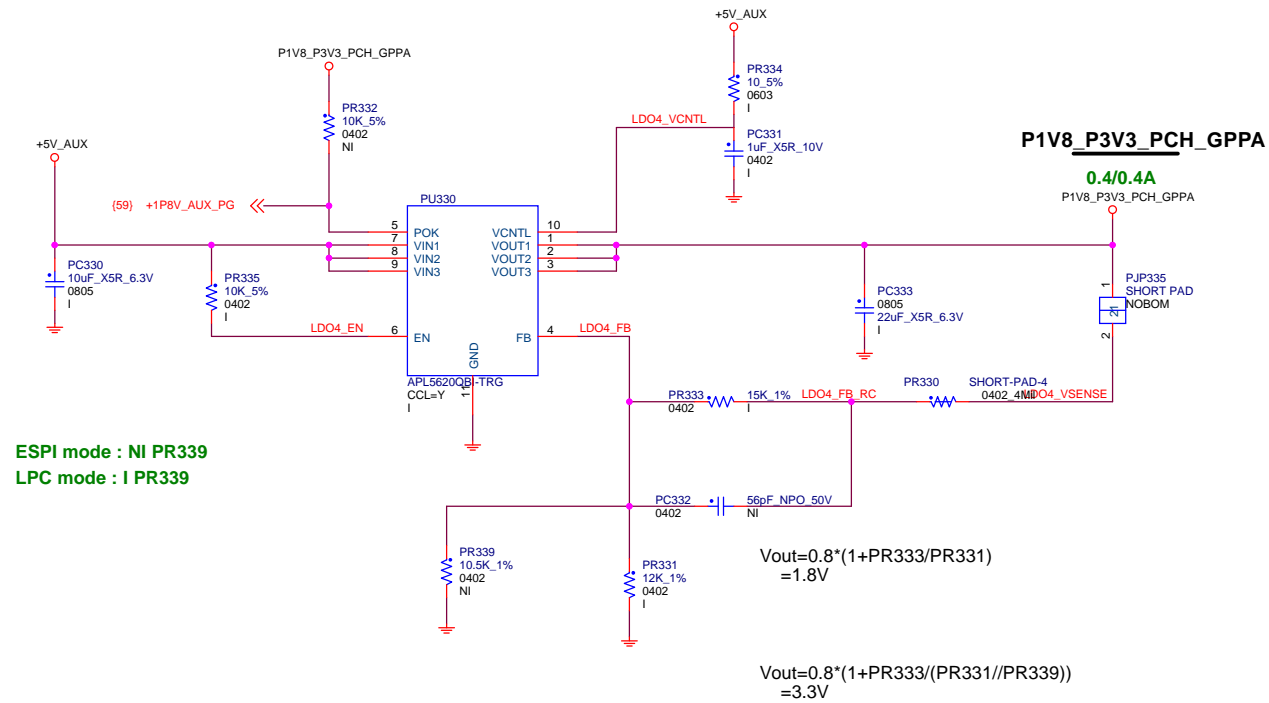


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Title +5V_GPIO					
Size	Document	Number			Rev
Custom	795207-000				A
Date: Monday, June 29, 2015				Sheet	57 of 72

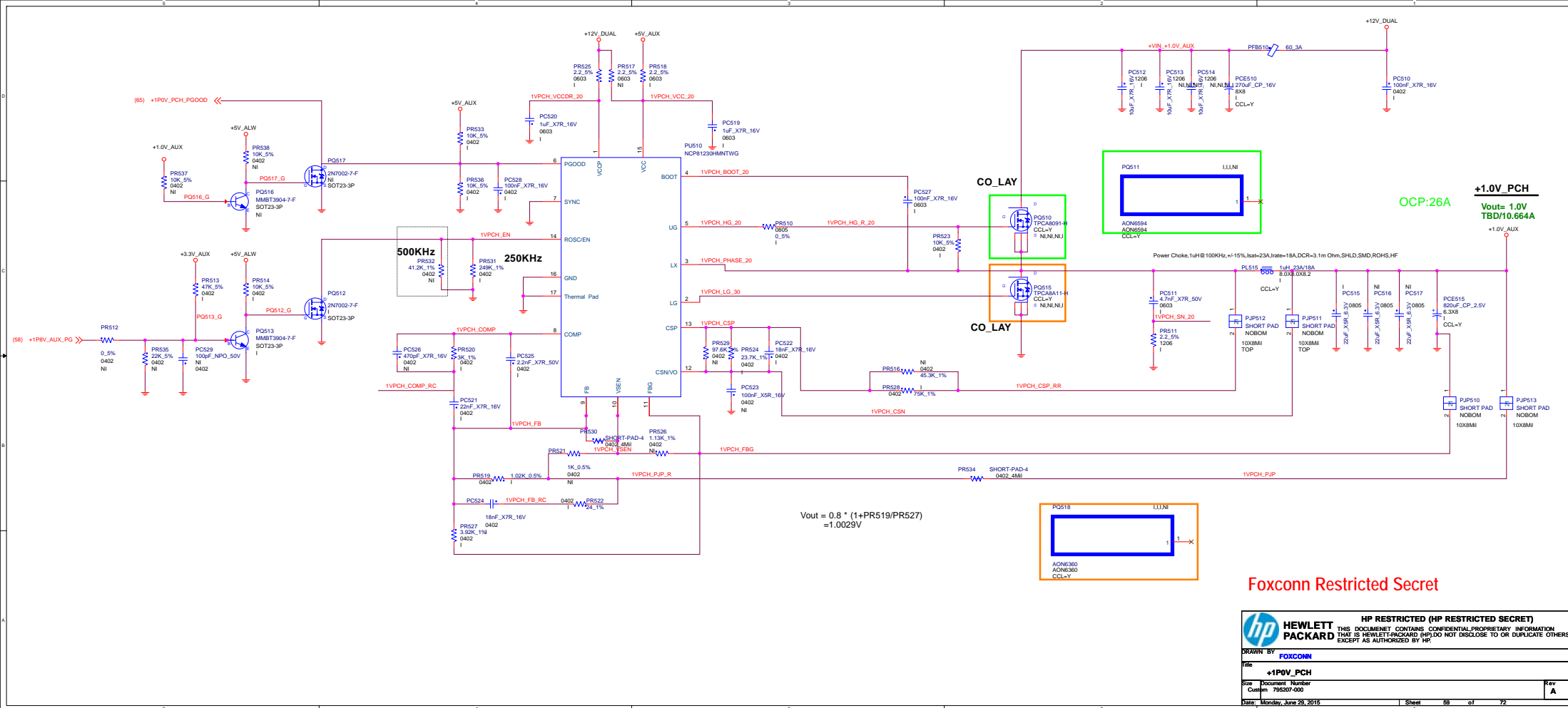
+1P8V_AUX

P1V8_P3V3_PCH_GPPA




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	DRAWN BY FOXCONN			
Title +1P8V_+3P3V_PCH_GPPA				
Size Custom	Document Number 795207-000			Rev A
Date: Monday, June 29, 2015	Sheet	58	of	72



1	2	3	4	5	6	7	8
A							
B							
C							
D							
1	2	3	4	5	6	7	8

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Title		BLANK			
Size	Document Number			Rev	
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PR570 set frequency
 $f_{sw} \text{ (KHz)} = 38000 \times V_o / R_{ton} \text{ (kohm)}$
 $= 500K$

If need in S4 should confirm with HP


+VPP
 $V_{out} = 2.5V$
 $TBD/2.24A$

PC579 should near XMM1

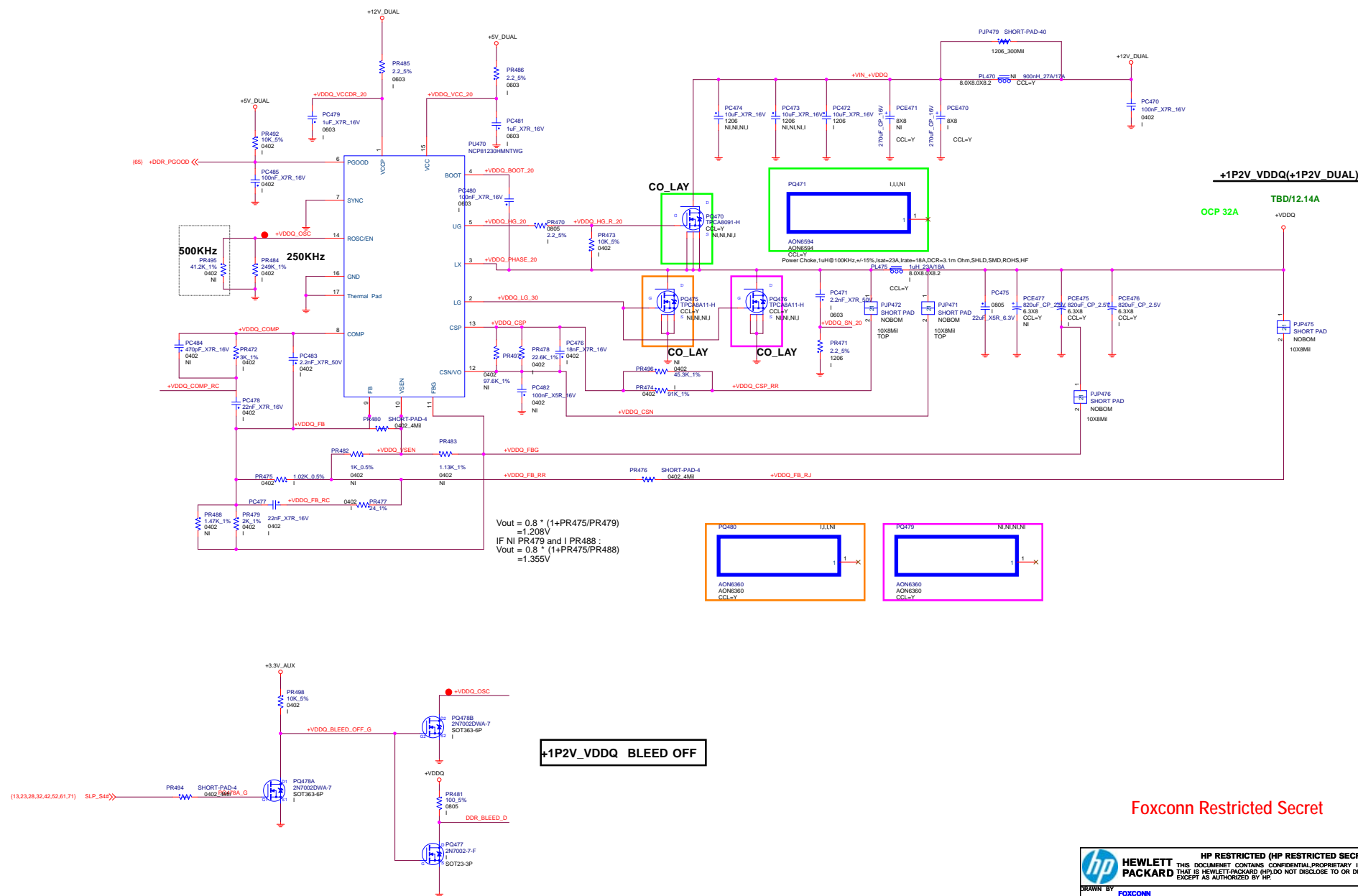
$V_{out} = 0.8 \times (1 + PR565/PR568)$
 $= 2.52V$

$V_{out} = 0.8 \times (1 + PR633/PR632)$
 $= 2.61V$

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DRAWN BY: FOXCONN			
Rev: +VPP			
Job Number: 785207-000		Rev: A	
Date: Monday, June 29, 2015		Sheet: 61 of 72	

+1P2V_VDDQ

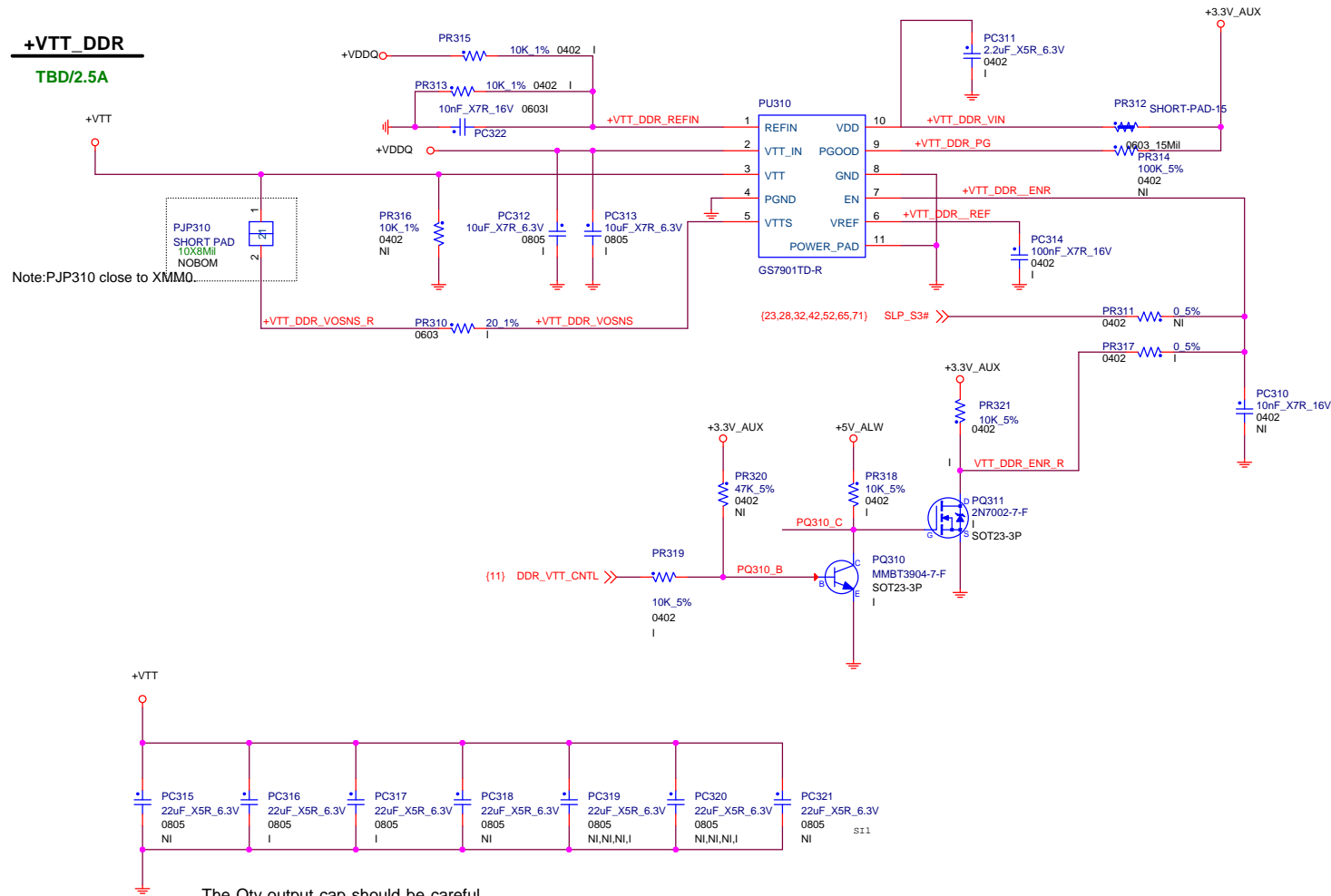


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DDR_VTT

+VTT_DDR

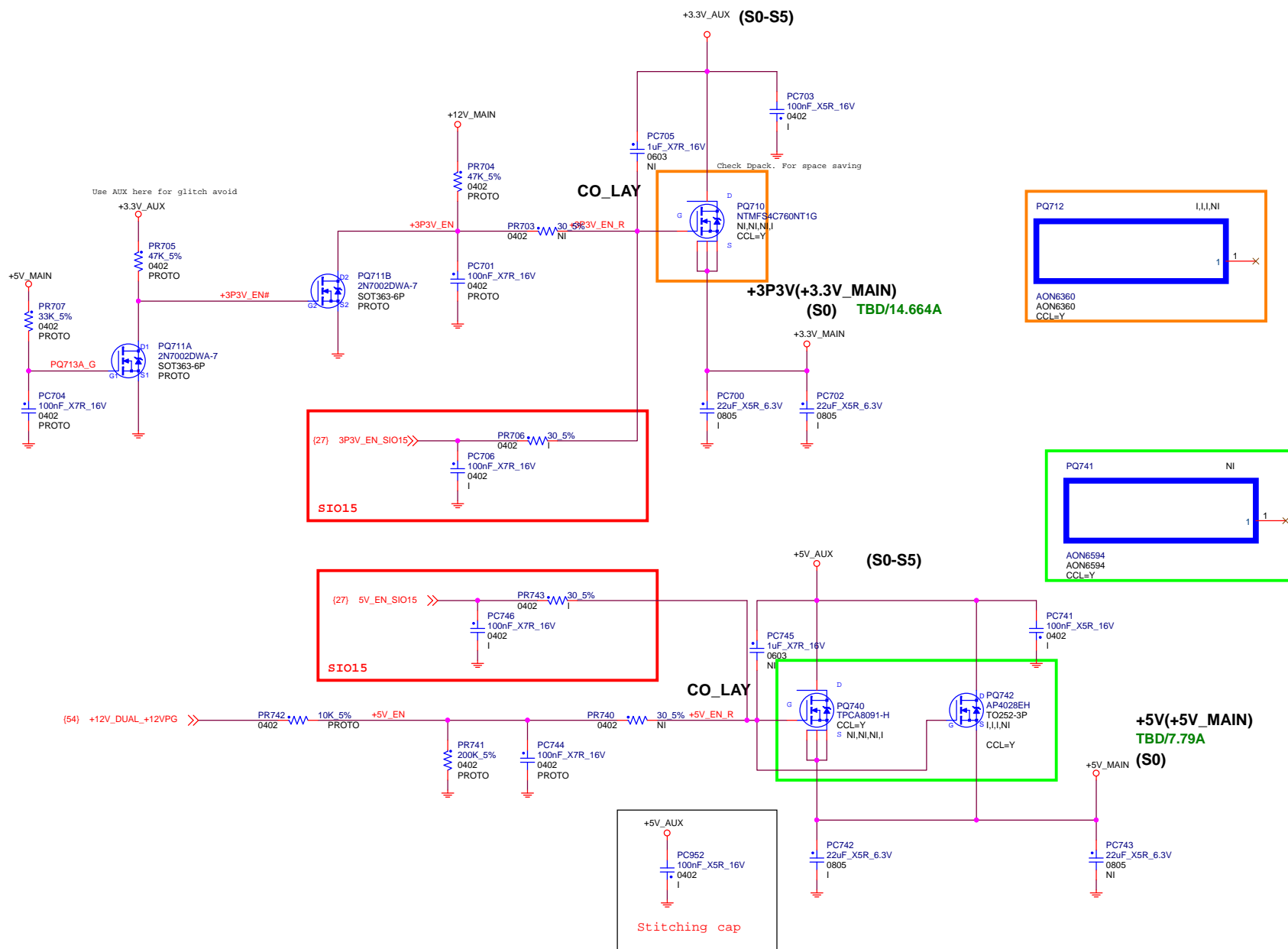
TBD/2.5A



The Qty output cap should be careful
INTEL: the latest modeling shows step load size 6-9x higher than it's shown in PDG
1.0 for Aztec City CRB

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DRAWN BY		FOXCONN	
Title		+VTT_DDR	
Size	Document Number	Rev	A
Date:	Tuesday, June 30, 2015	Sheet	63 of 72

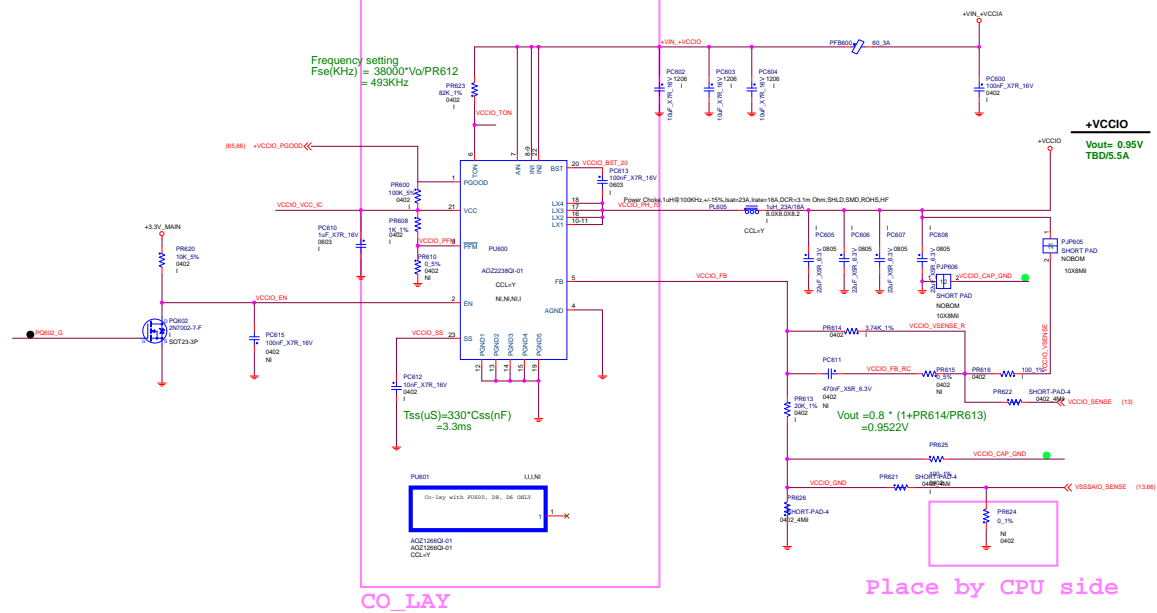


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DRAWN BY FOXCONN			
Title +5V_MAIN & +3P3V_MAIN			
Size Document Number Custom 795207-000	Date: Monday, June 29, 2015		Rev A
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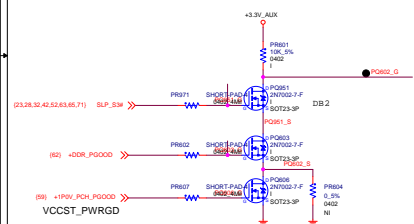
+VCCIO

Frequency setting
Fse(KHz)
= 38000*Vo/PR612
= 493KHz

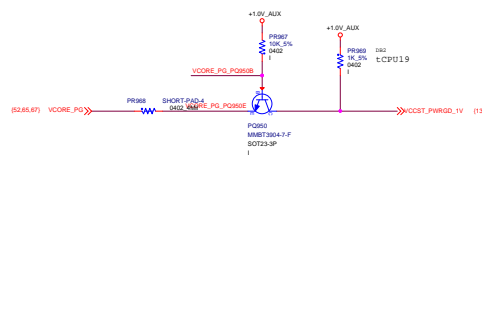
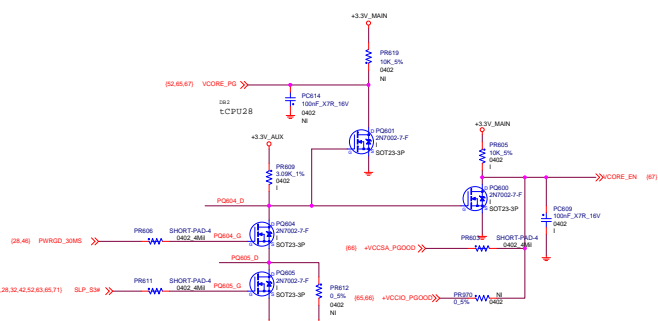


CO_LAY

Place by CPU side

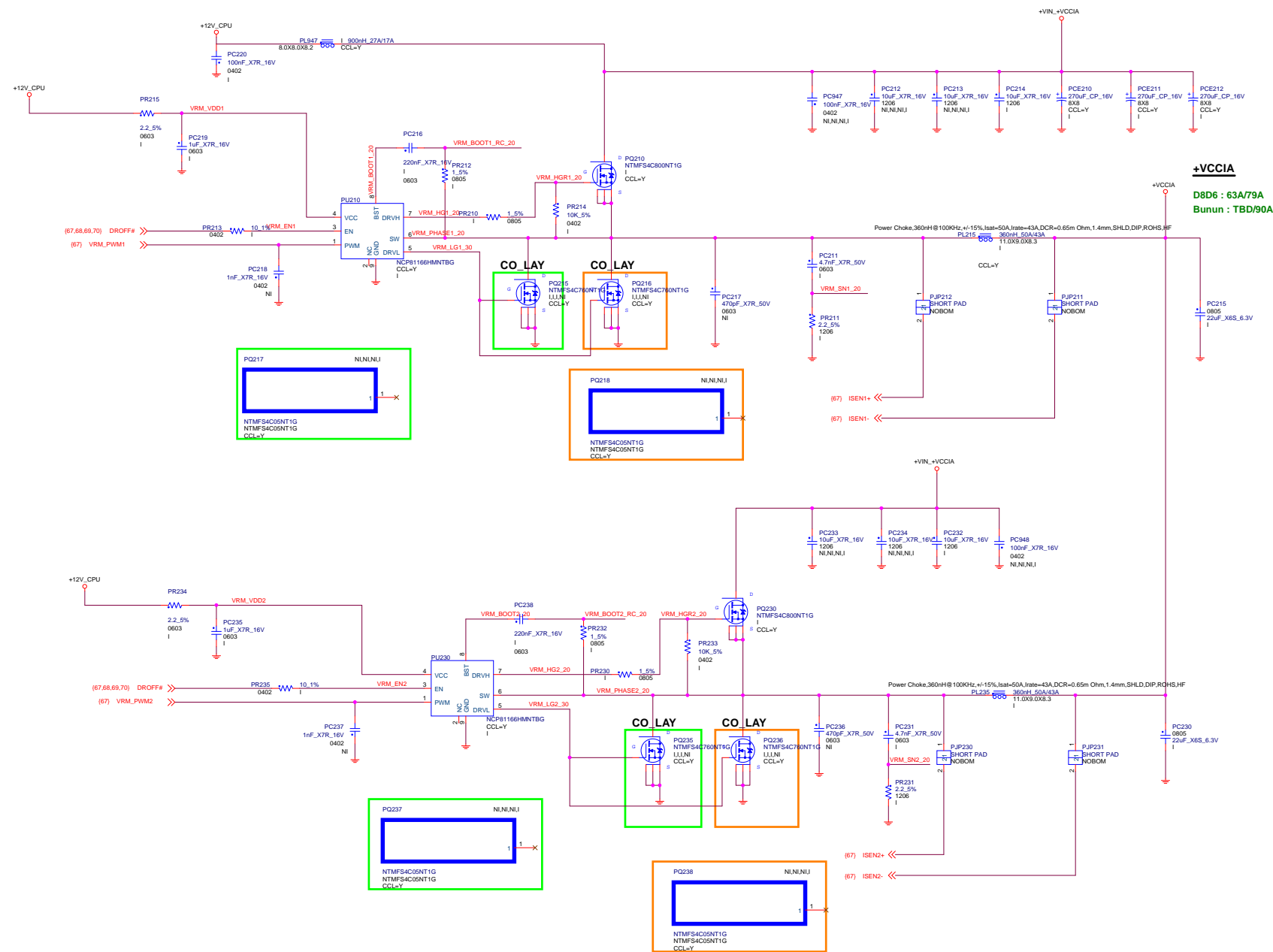


VCCST_PWRGD



FOXCONN Restricted Secret.

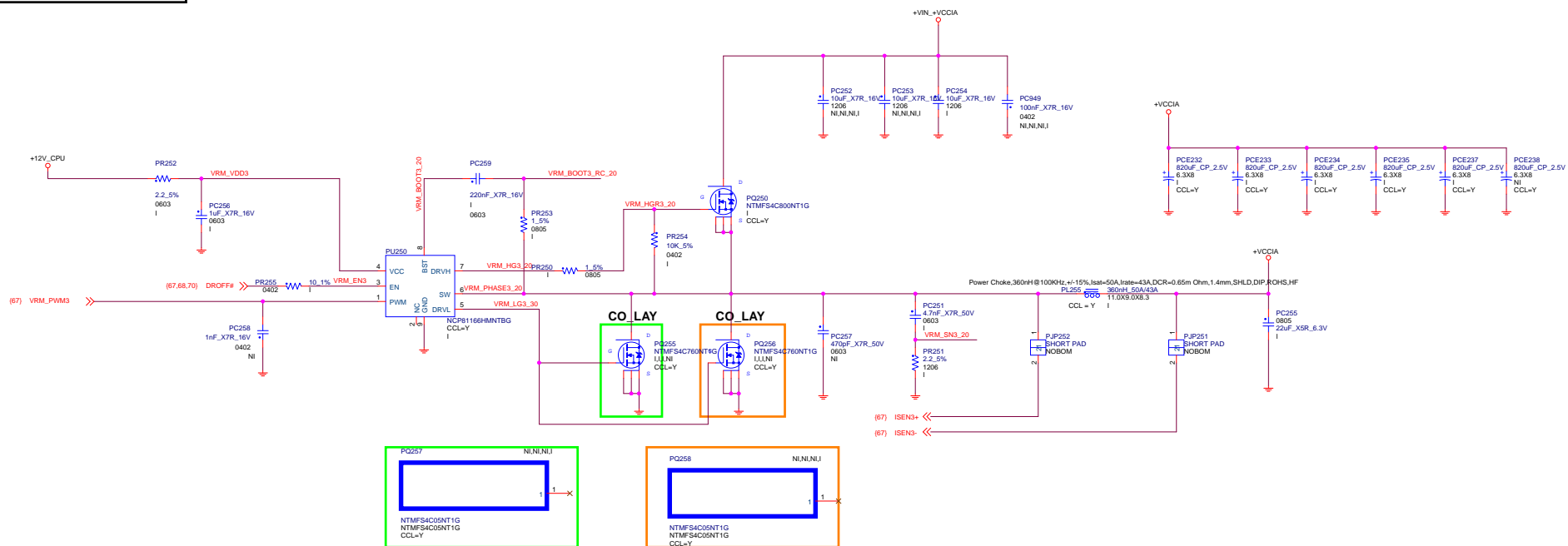
VCORE PHASE1~2



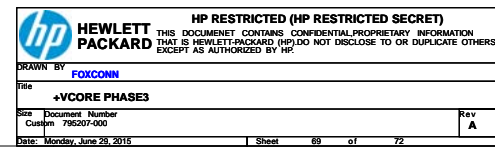
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DRAWN BY: FOXCONN			
File: +VCORE PHASE 1 & 2			
Site:	Document Number:	Rev: A	
Custom:	796207-000		
Date:	Monday, June 29, 2015	Sheet:	68 of 72

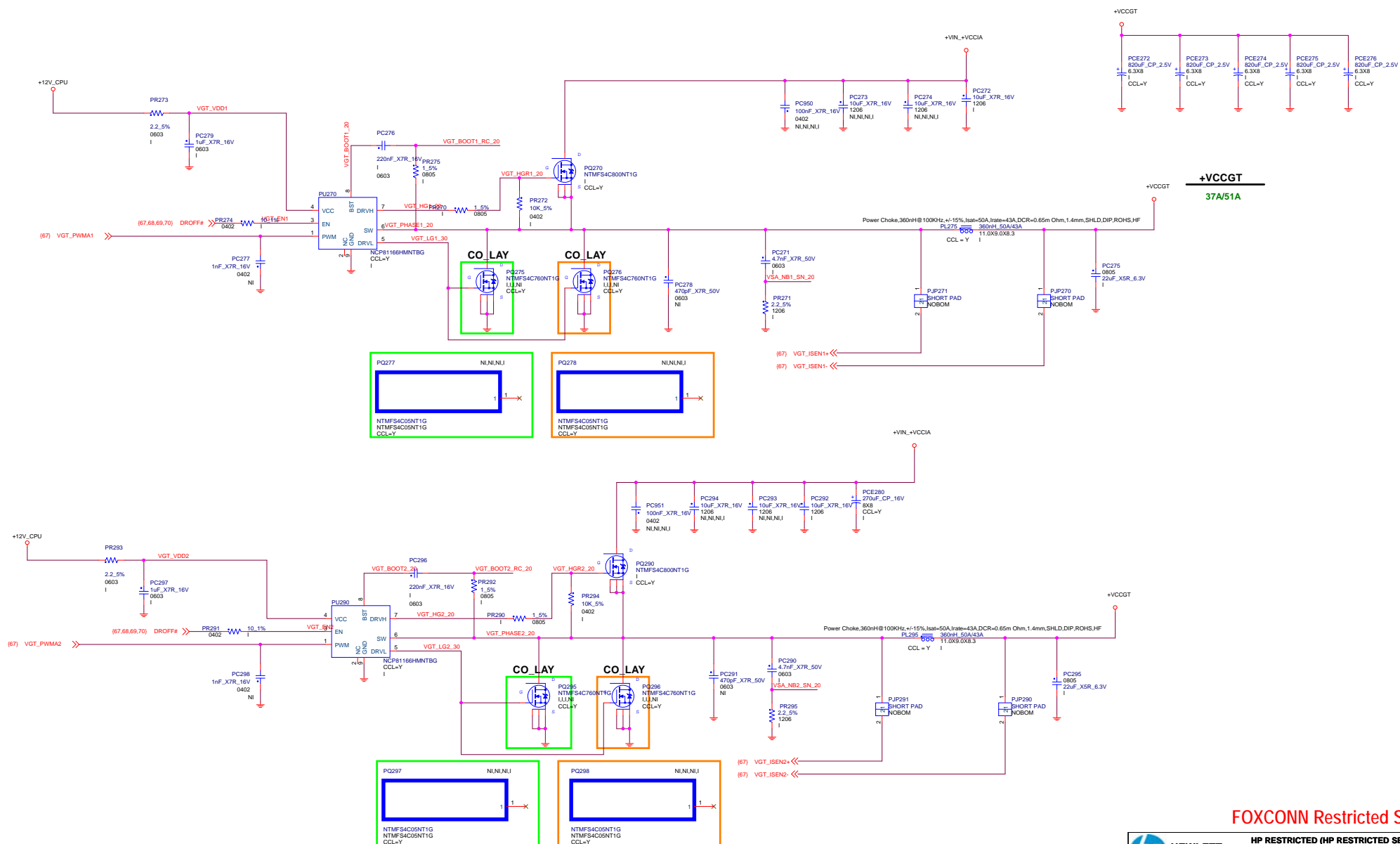
VCORE PHASE3



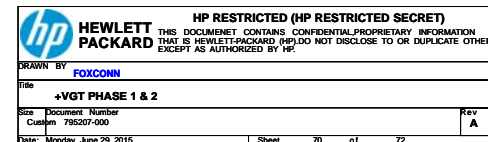
FOXCONN Restricted Secret.



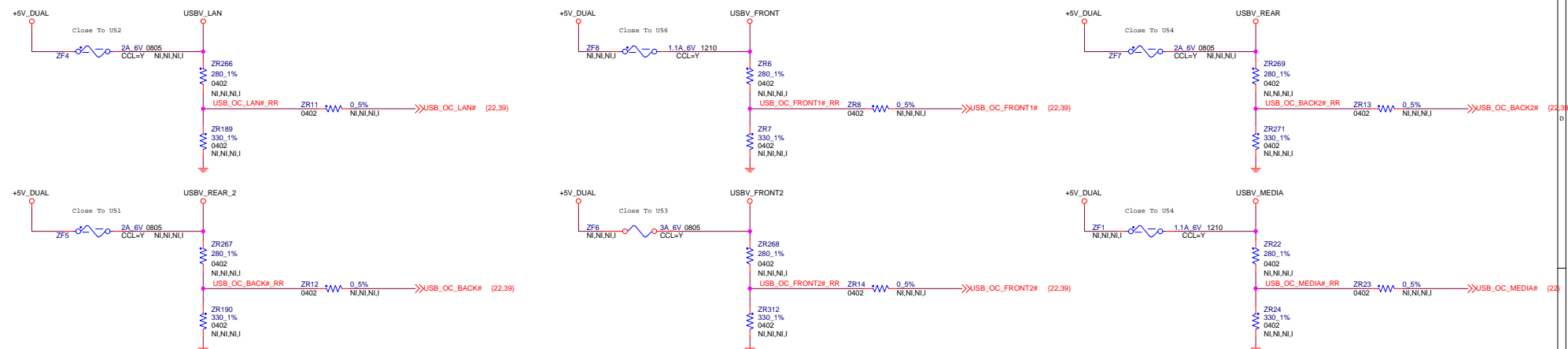
VGT PHASE1~2



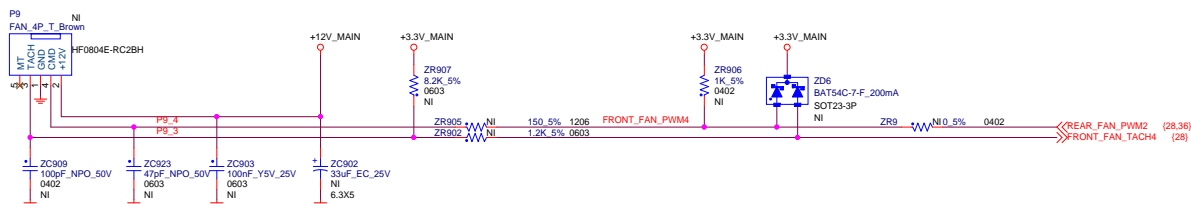
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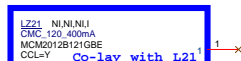
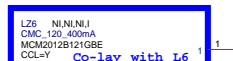
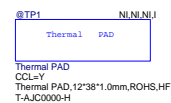
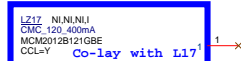
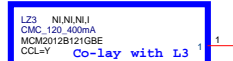
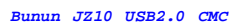
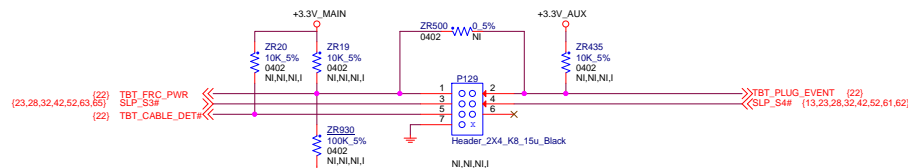
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